

Model Name:GA-F2A85X-UP4

Component value change history

Version: 1.01

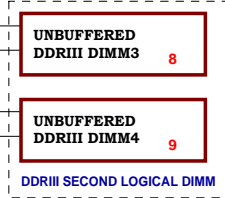
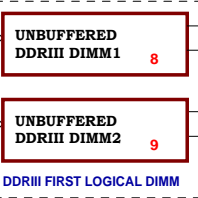
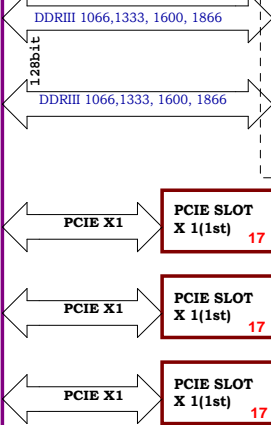
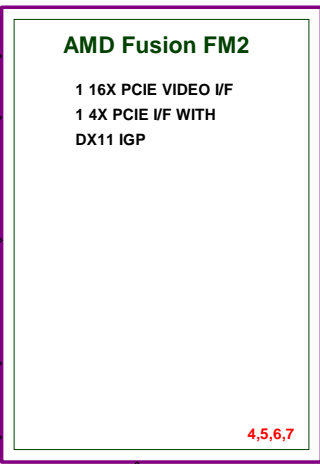
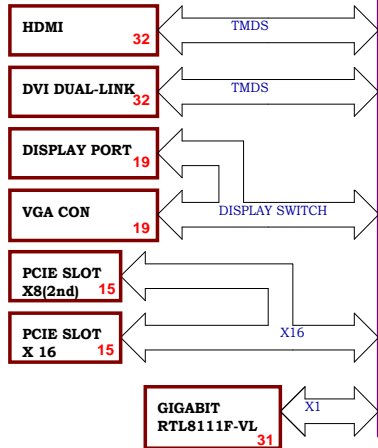
P-Code: U12033-0
9MF285XP4-00

[illegible]

Circuit or PCB layout change for next version

[illegible]

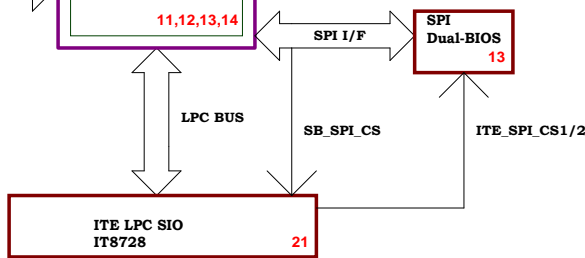
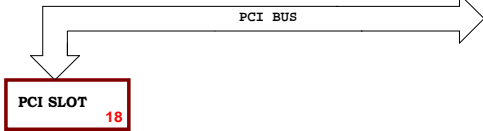
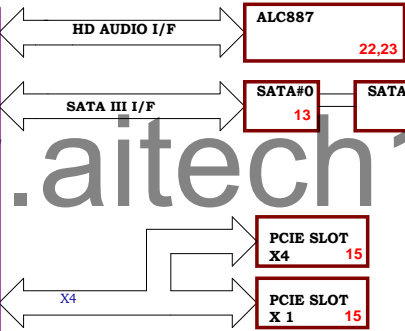
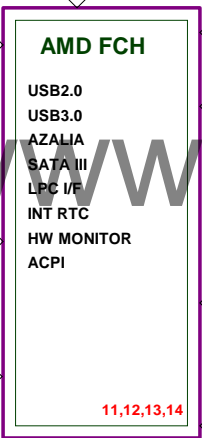
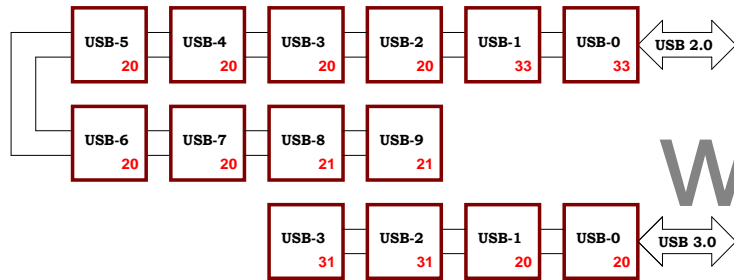
Clock
Generator
9LPR4850 10



APU POWER
IR3567 + IR3598
27,28

DDR3 MEMORY POWER
RT8120
29

Fusion A85 CORE &
PCIE POWER
RT8120
30



GIGABYTE

Title
BLOCK DIAGRAM

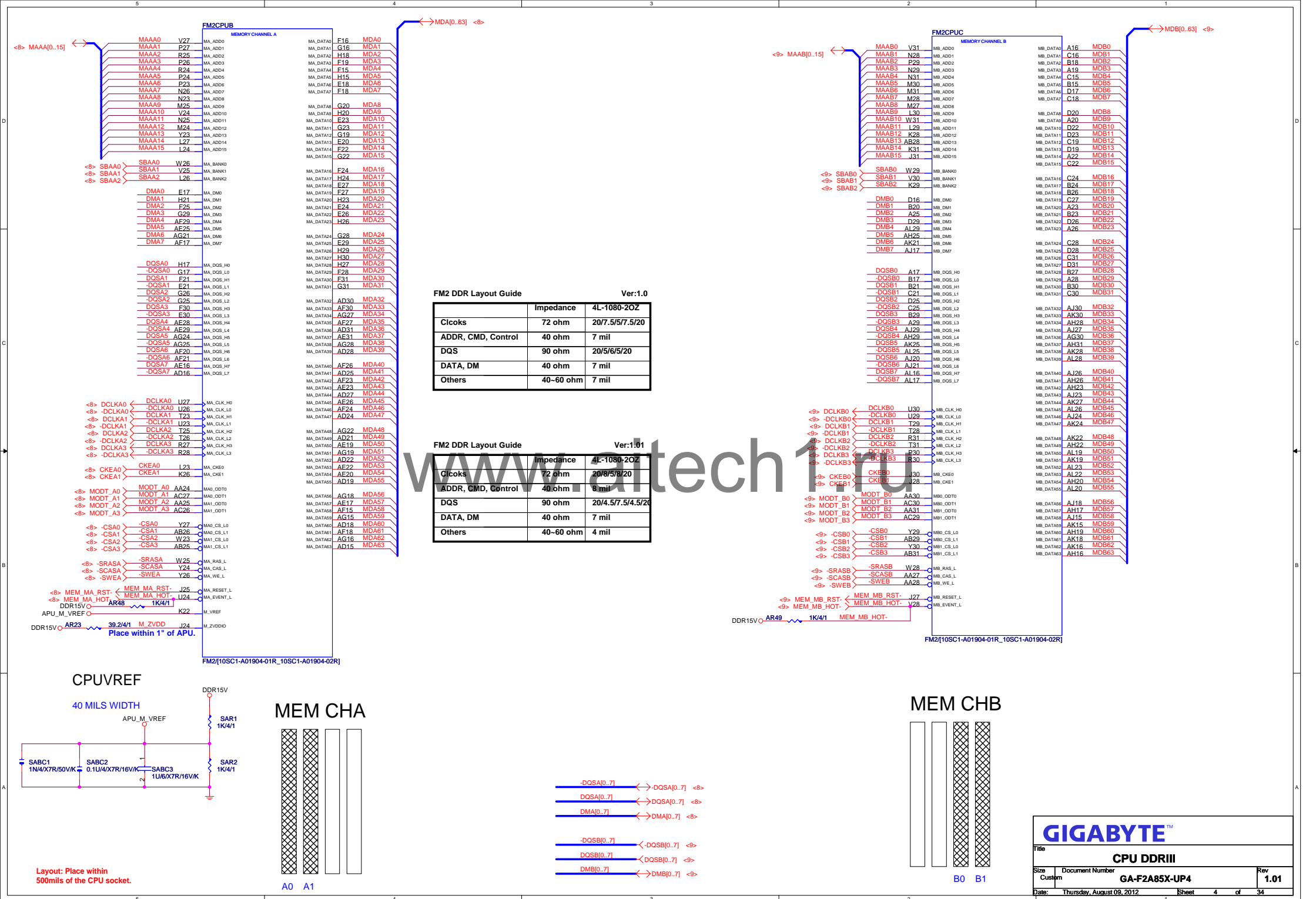
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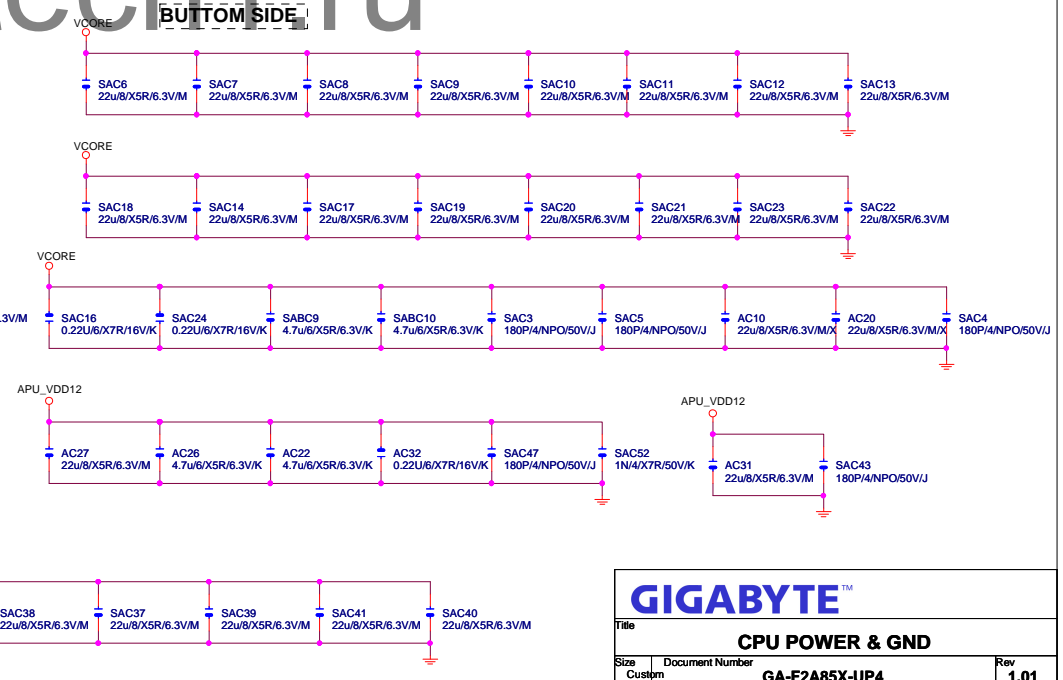
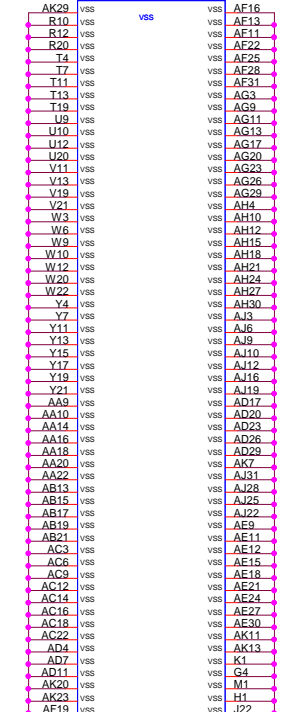
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GA-F2A85X-UP4

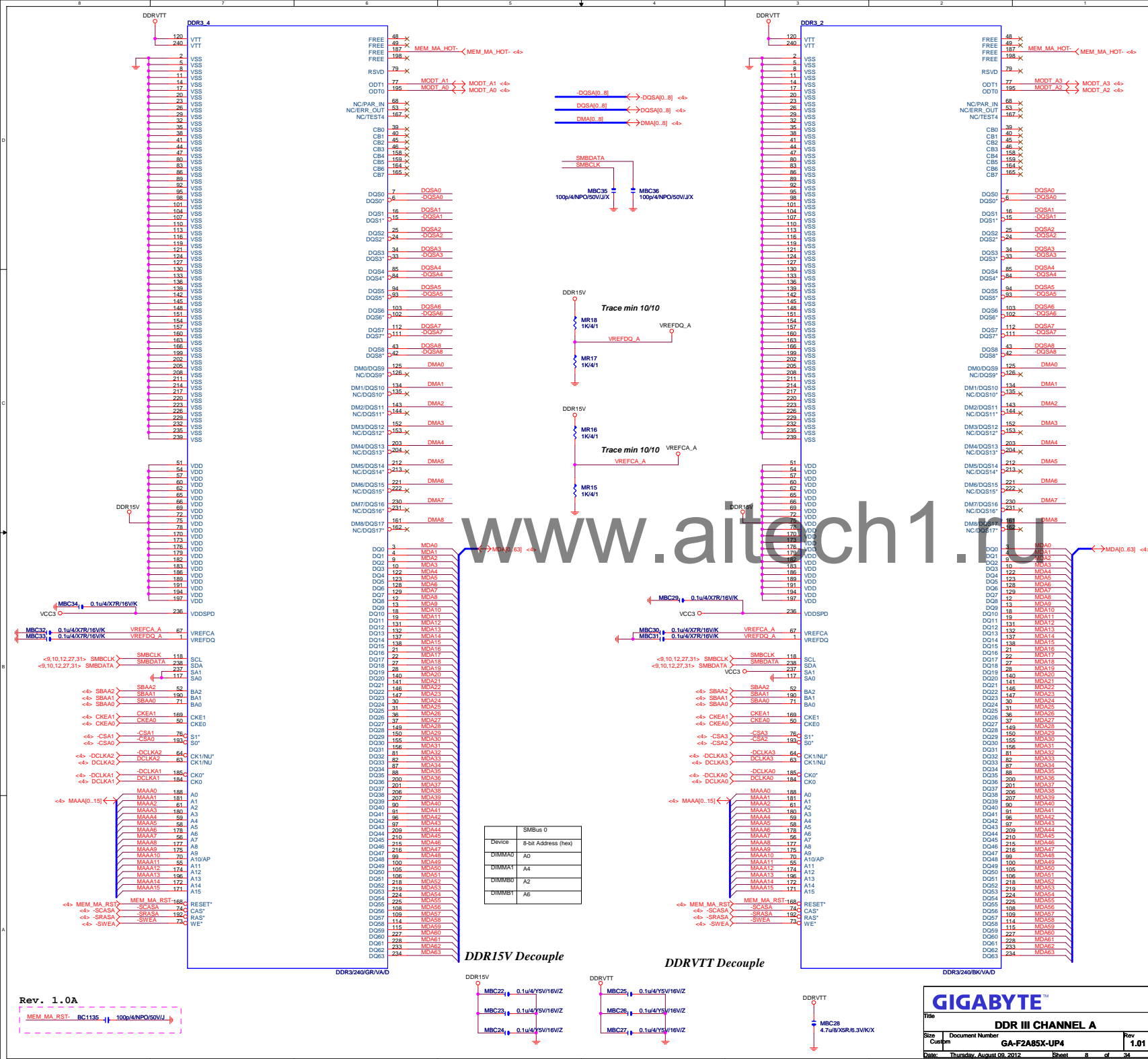
Rev
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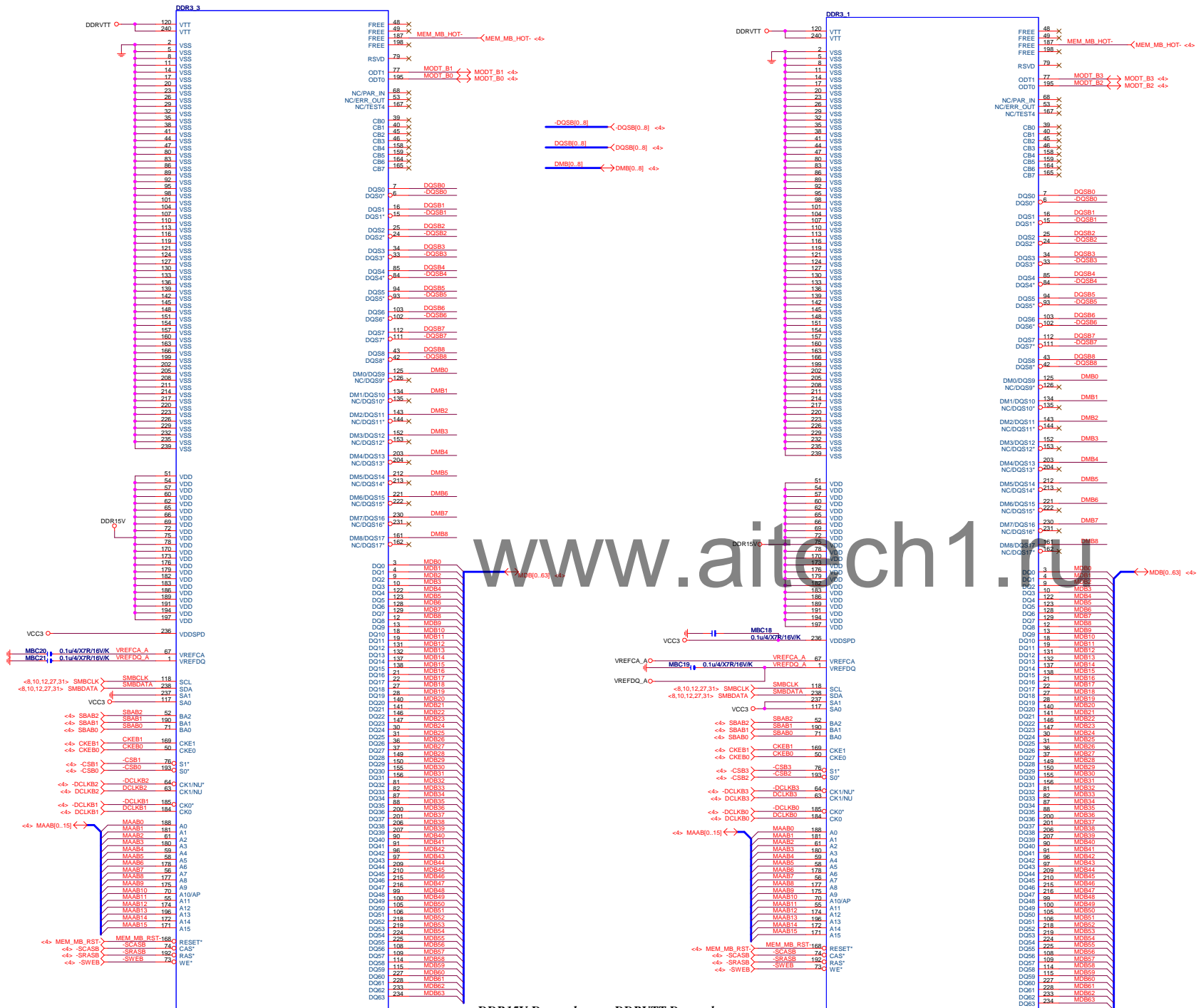
Date: Thursday, August 09, 2012

Sheet 3 of 34

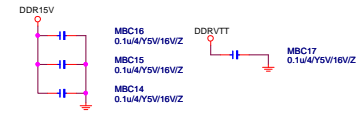








DDR15V Decouple DDRVTT Decouple



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Title

DDR III CHANNEL B

Size

Document Number

GA-F2A85X-UP4

Rev

1.01

Date

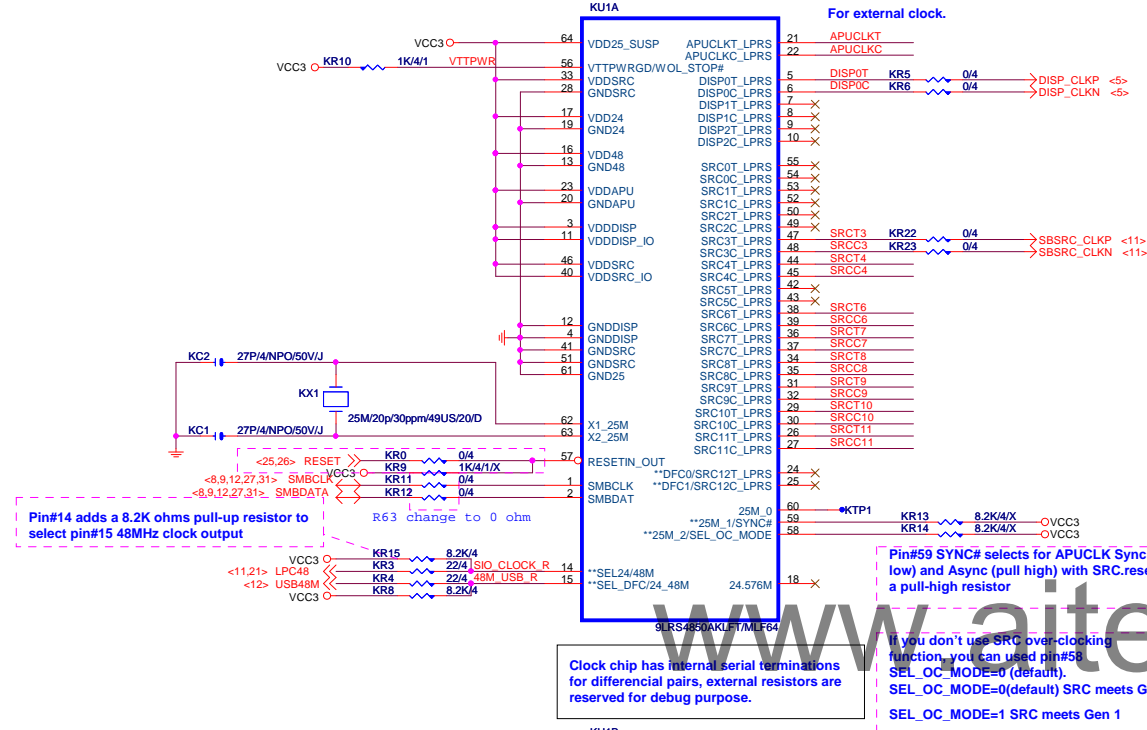
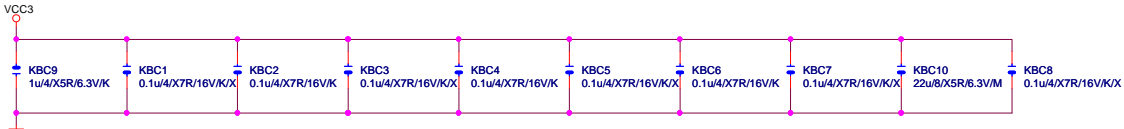
Thursday, August 09, 2012

Sheet

9

of

34



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

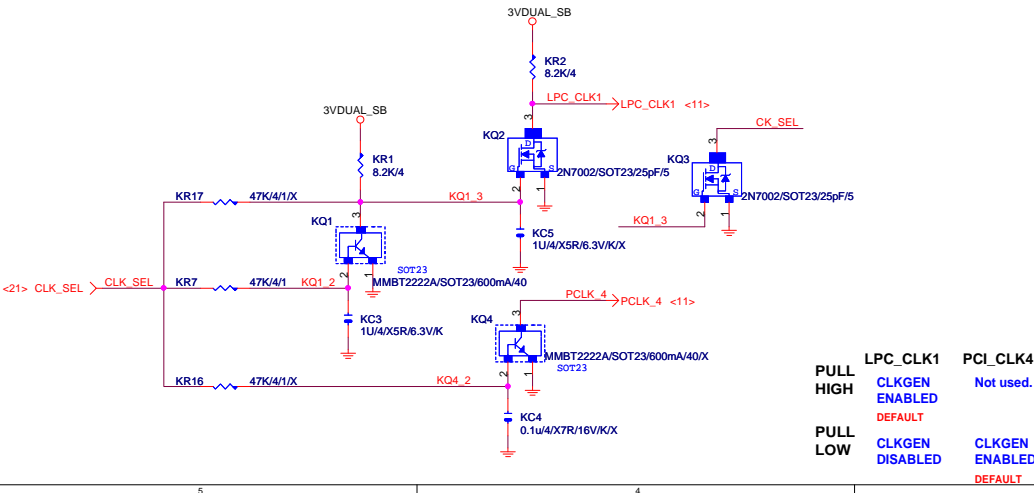
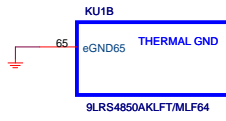
Pin#59 SYNC# selects for APUCCLK Sync (pull low) and Async (pull high) with SRC.reserve a pull-high resistor

If you don't use SRC over-clocking function, you can use pin#58

SEL_OC_MODE=0 (default)

SEL_OC_MODE=0 (default) SRC meets Gen 2

SEL_OC_MODE=1 SRC meets Gen 1



LPC_CLK1 CLKGEN ENABLED

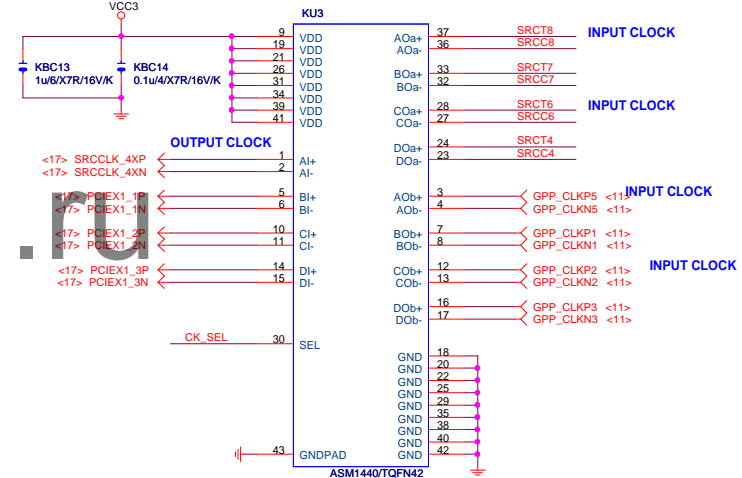
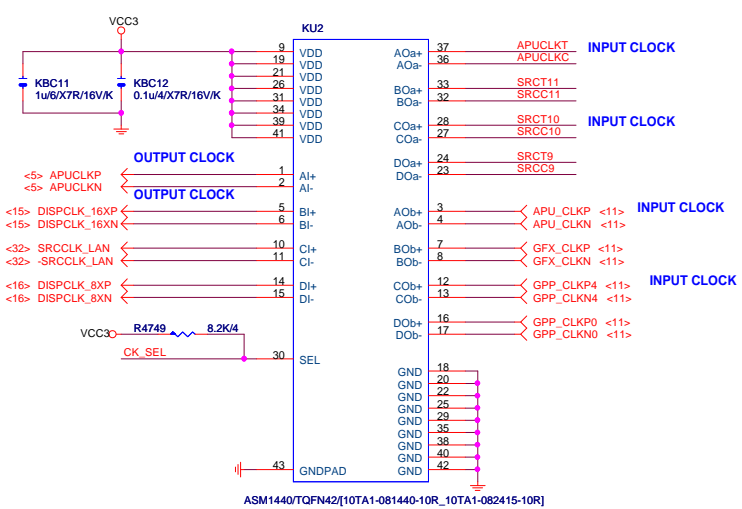
PCI_CLK4 Not used.

CLKGEN ENABLED

CLKGEN DISABLED

CLKGEN ENABLED

CLKGEN DISABLED



Function	SEL	CLK source
x1-> xOa	L	External
x1-> xOb	H	Internal

Title

Size

Date

Document Number

Customer

Thursday, August 09, 2012

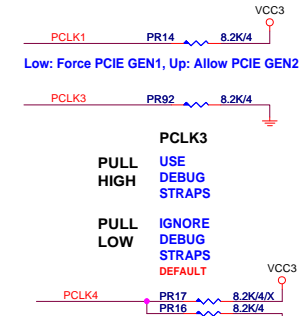
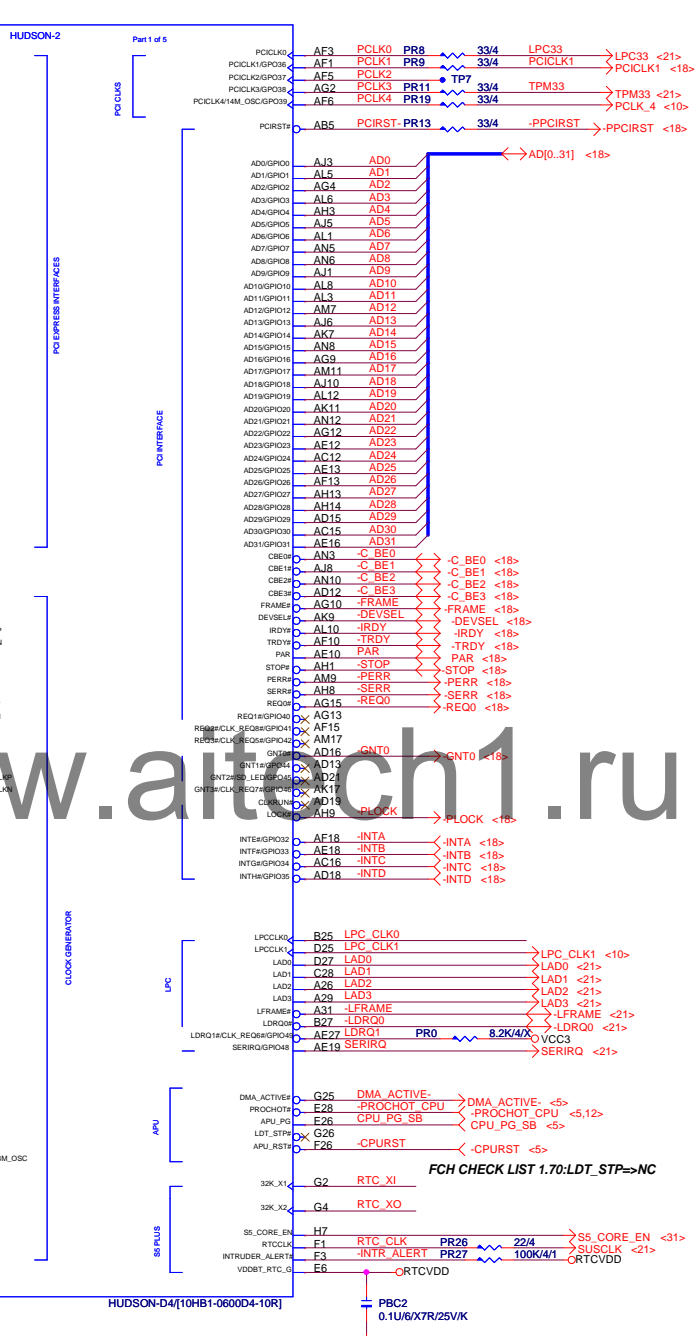
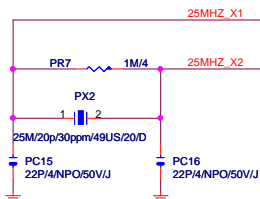
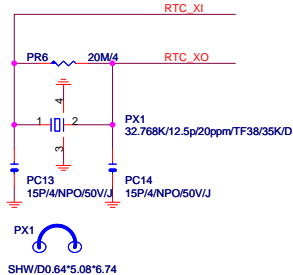
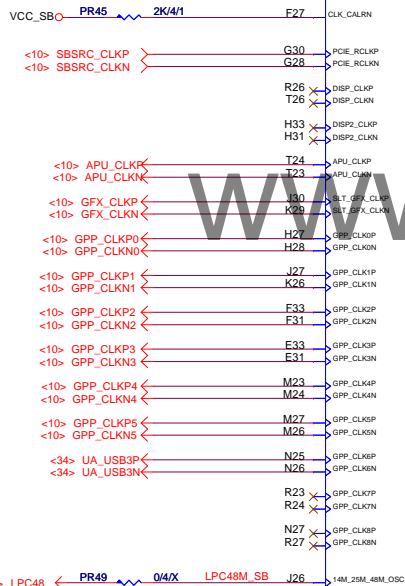
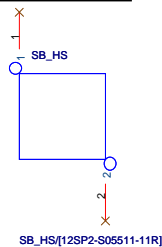
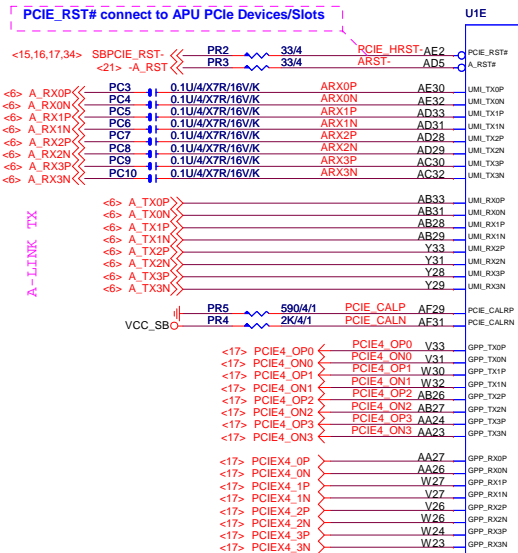
Rev

1.01

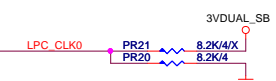
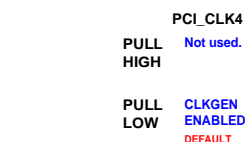
Sheet 10 of 34



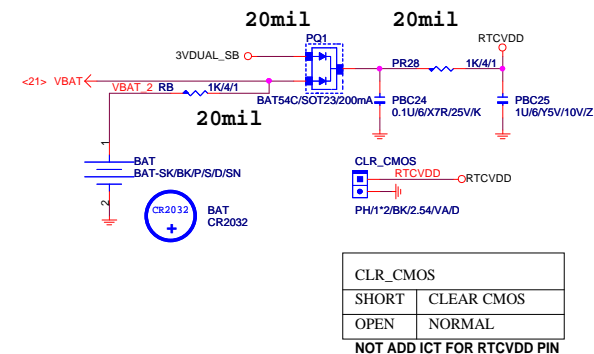
A-LINK RX



APU_CLKP/N and DISP_CLKP/N Clock Selection
0V Required setting for integrated clock mode.
3.3V Reserved. This strap is not used if the strap CLKGEN is configured for external clock generator mode.



	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	IMC DISABLED	CLKGEN DISABLED
	DEFAULT	DEFAULT

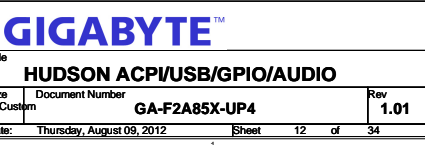


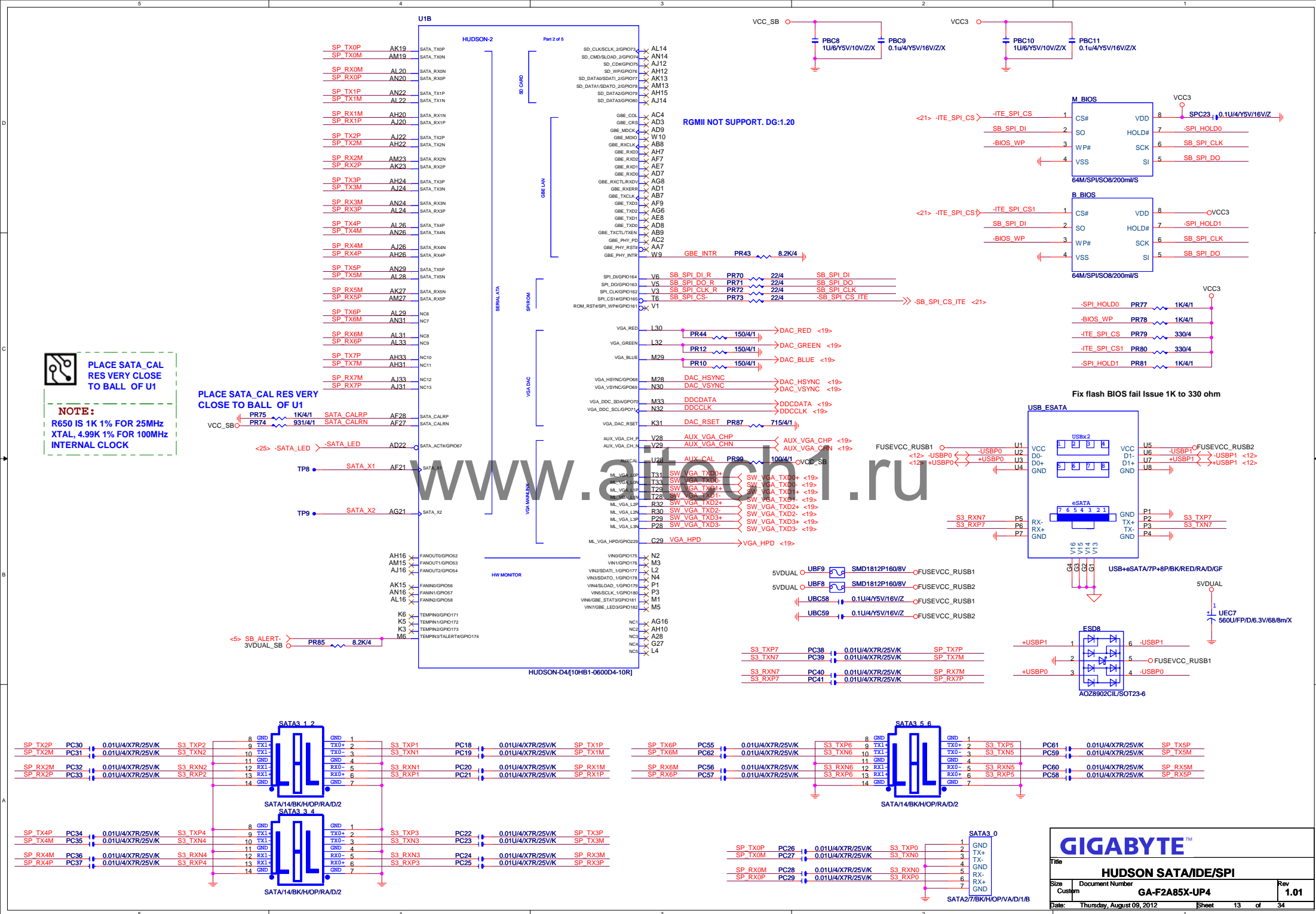
NOT ADD ICT FOR RTCVDD PIN

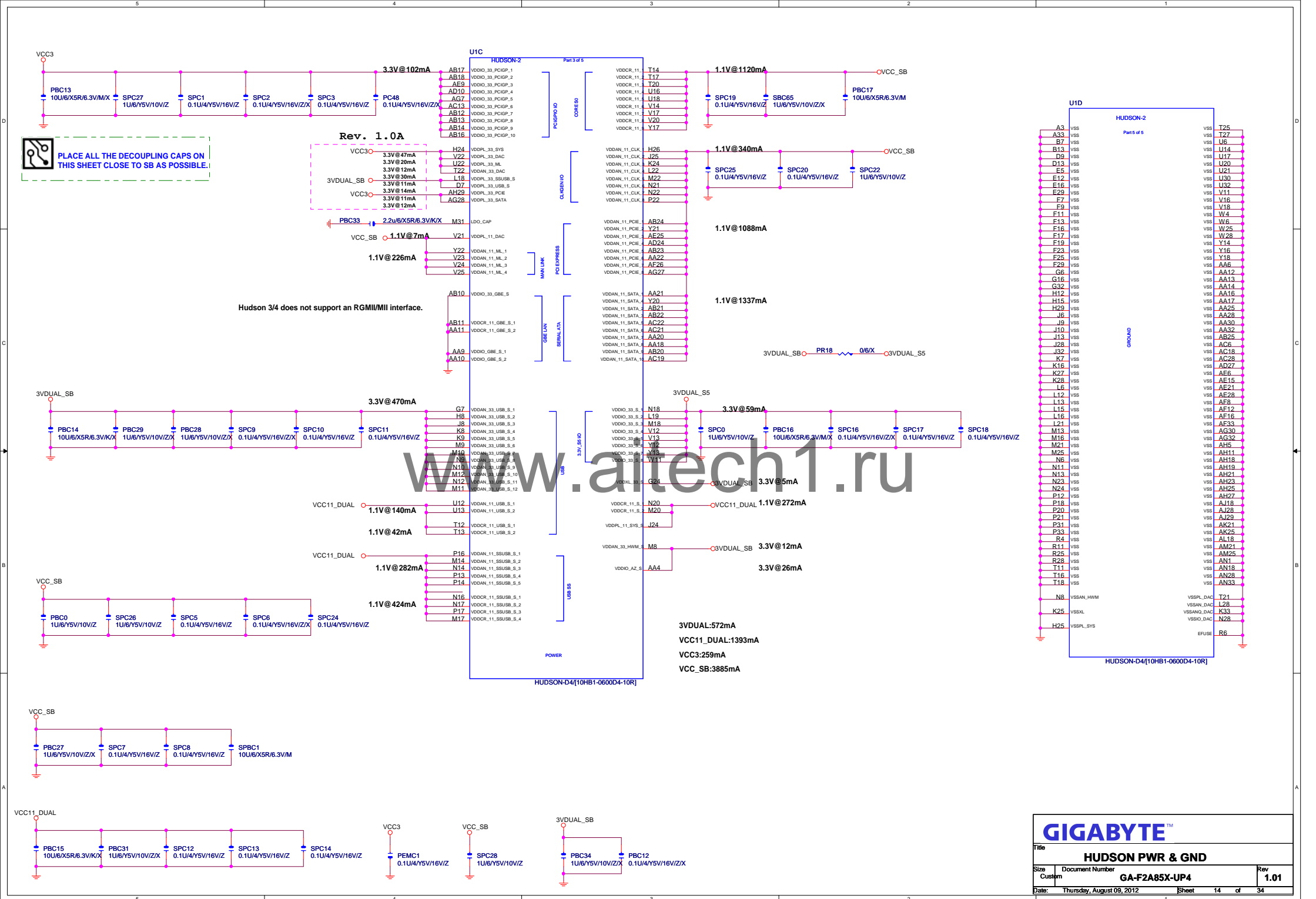
GIGABYTE

Title			
HUDSON PCIE/PCI/CPU/LPC			
Size	Document Number	Rev	
Custom	GA-F2A85X-UP4	1.01	
Date:	Thursday, August 09, 2012	Sheet	11 of 34

Disable: 10K pull-up to +3.3V_S5.
Enable: 2.2K pull-down.

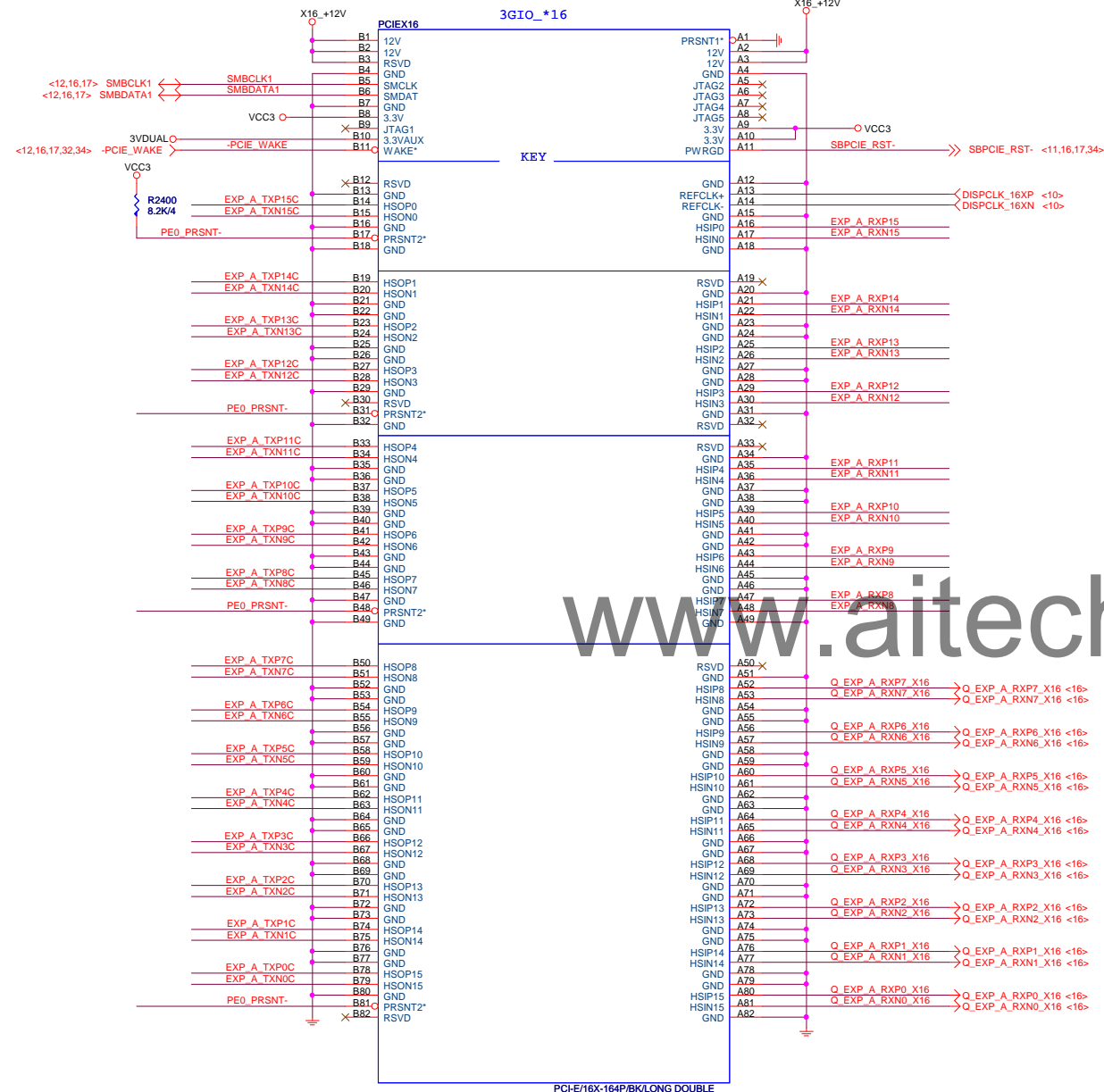
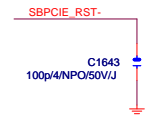
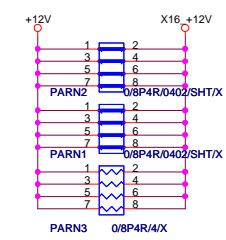




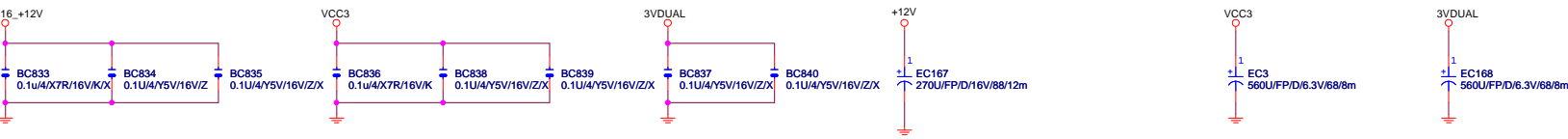


EXP_A_RXP[8..15] >> EXP_A_RXP[8..15] << EXP_A_TXP[8..15] >> EXP_A_TXP[8..15]
EXP_A_RXN[8..15] >> EXP_A_RXN[8..15] << EXP_A_TXN[8..15] >> EXP_A_TXN[8..15]

Rev. 1.01A



<16> Q_EXP_A_TXP0_X16	C1644	0.1U4/X7R/16V/K	EXP_A_TXP0C
<16> Q_EXP_A_TXN0_X16	C1645	0.1U4/X7R/16V/K	EXP_A_TXN0C
<16> Q_EXP_A_TXP1_X16	C1646	0.1U4/X7R/16V/K	EXP_A_TXP1C
<16> Q_EXP_A_TXN1_X16	C1647	0.1U4/X7R/16V/K	EXP_A_TXN1C
<16> Q_EXP_A_TXP2_X16	C1648	0.1U4/X7R/16V/K	EXP_A_TXP2C
<16> Q_EXP_A_TXN2_X16	C1649	0.1U4/X7R/16V/K	EXP_A_TXN2C
<16> Q_EXP_A_TXP3_X16	C1650	0.1U4/X7R/16V/K	EXP_A_TXP3C
<16> Q_EXP_A_TXN3_X16	C1651	0.1U4/X7R/16V/K	EXP_A_TXN3C
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<16> Q_EXP_A_TXN4_X16	C1653	0.1U4/X7R/16V/K	EXP_A_TXN4C
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<16> Q_EXP_A_TXN6_X16	C1657	0.1U4/X7R/16V/K	EXP_A_TXN6C
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<16> Q_EXP_A_TXN7_X16	C1659	0.1U4/X7R/16V/K	EXP_A_TXN7C
EXP_A_TXP8	C1660	0.1U4/X7R/16V/K	EXP_A_TXP8C
EXP_A_TXN8	C1661	0.1U4/X7R/16V/K	EXP_A_TXN8C
EXP_A_TXP9	C1662	0.1U4/X7R/16V/K	EXP_A_TXP9C
EXP_A_TXN9	C1663	0.1U4/X7R/16V/K	EXP_A_TXN9C
EXP_A_TXP10	C1664	0.1U4/X7R/16V/K	EXP_A_TXP10C
EXP_A_TXN10	C1665	0.1U4/X7R/16V/K	EXP_A_TXN10C
EXP_A_TXP11	C1666	0.1U4/X7R/16V/K	EXP_A_TXP11C
EXP_A_TXN11	C1667	0.1U4/X7R/16V/K	EXP_A_TXN11C
EXP_A_TXP12	C1668	0.1U4/X7R/16V/K	EXP_A_TXP12C
EXP_A_TXN12	C1669	0.1U4/X7R/16V/K	EXP_A_TXN12C
EXP_A_TXP13	C1670	0.1U4/X7R/16V/K	EXP_A_TXP13C
EXP_A_TXN13	C1671	0.1U4/X7R/16V/K	EXP_A_TXN13C
EXP_A_TXP14	C1672	0.1U4/X7R/16V/K	EXP_A_TXP14C
EXP_A_TXN14	C1673	0.1U4/X7R/16V/K	EXP_A_TXN14C
EXP_A_TXP15	C1674	0.1U4/X7R/16V/K	EXP_A_TXP15C
EXP_A_TXN15	C1675	0.1U4/X7R/16V/K	EXP_A_TXN15C



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Title
PCI EXPRESS X 16

Size
Custom

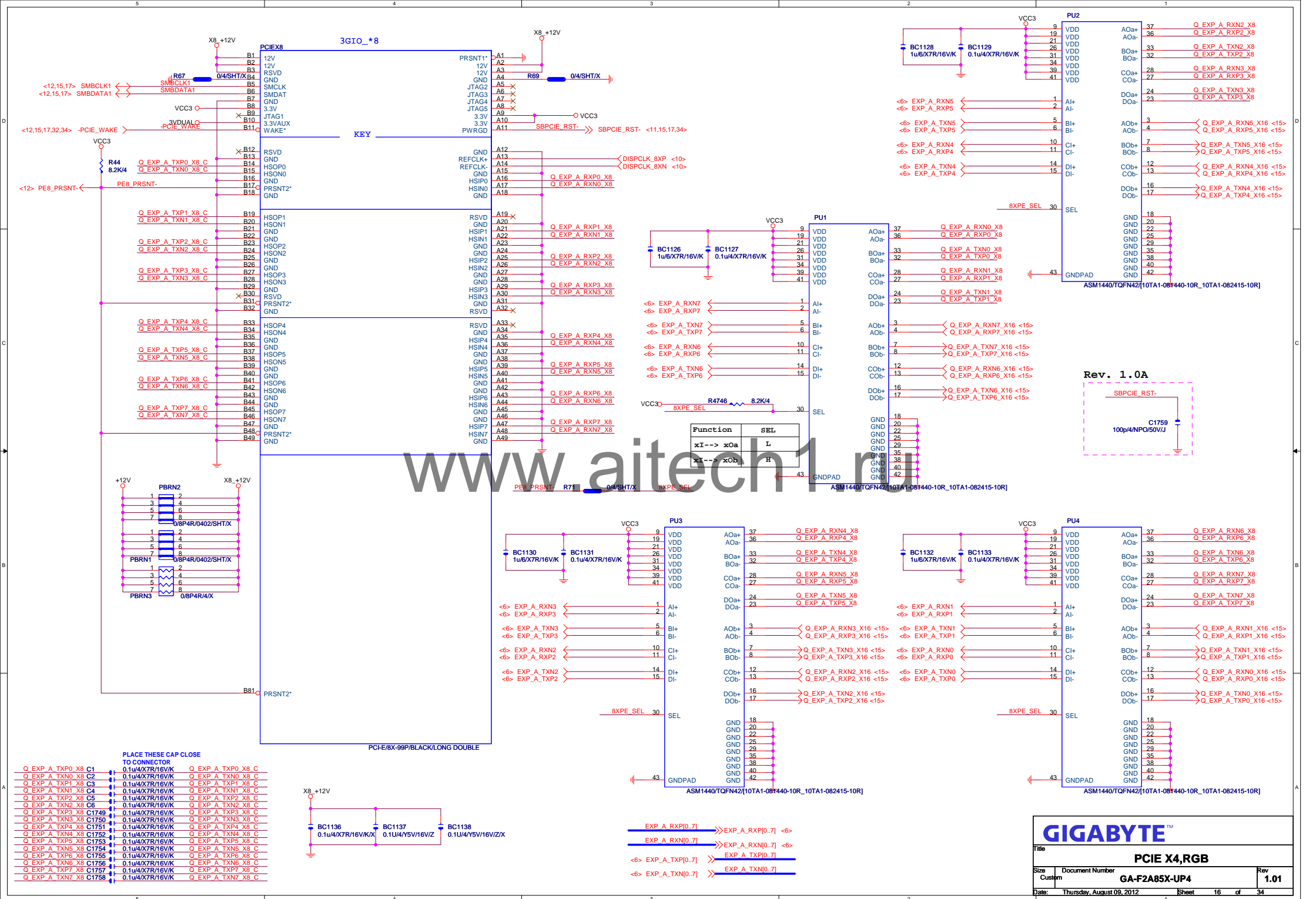
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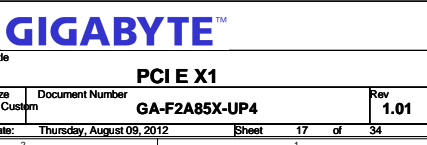
Rev
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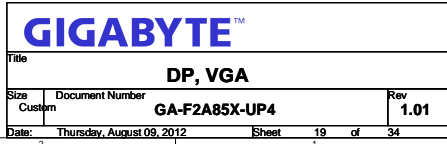
Date
Thursday, August 09, 2012

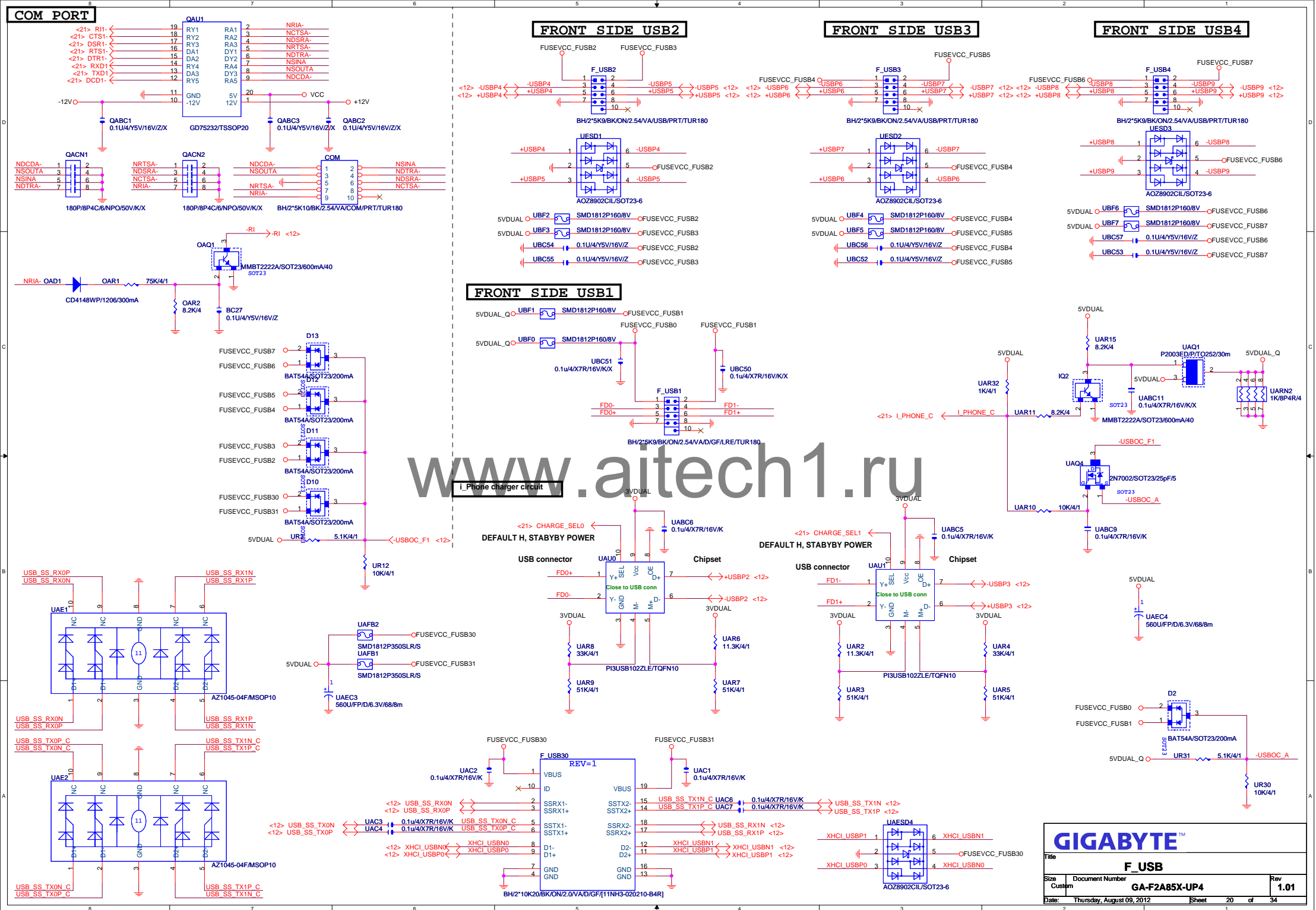
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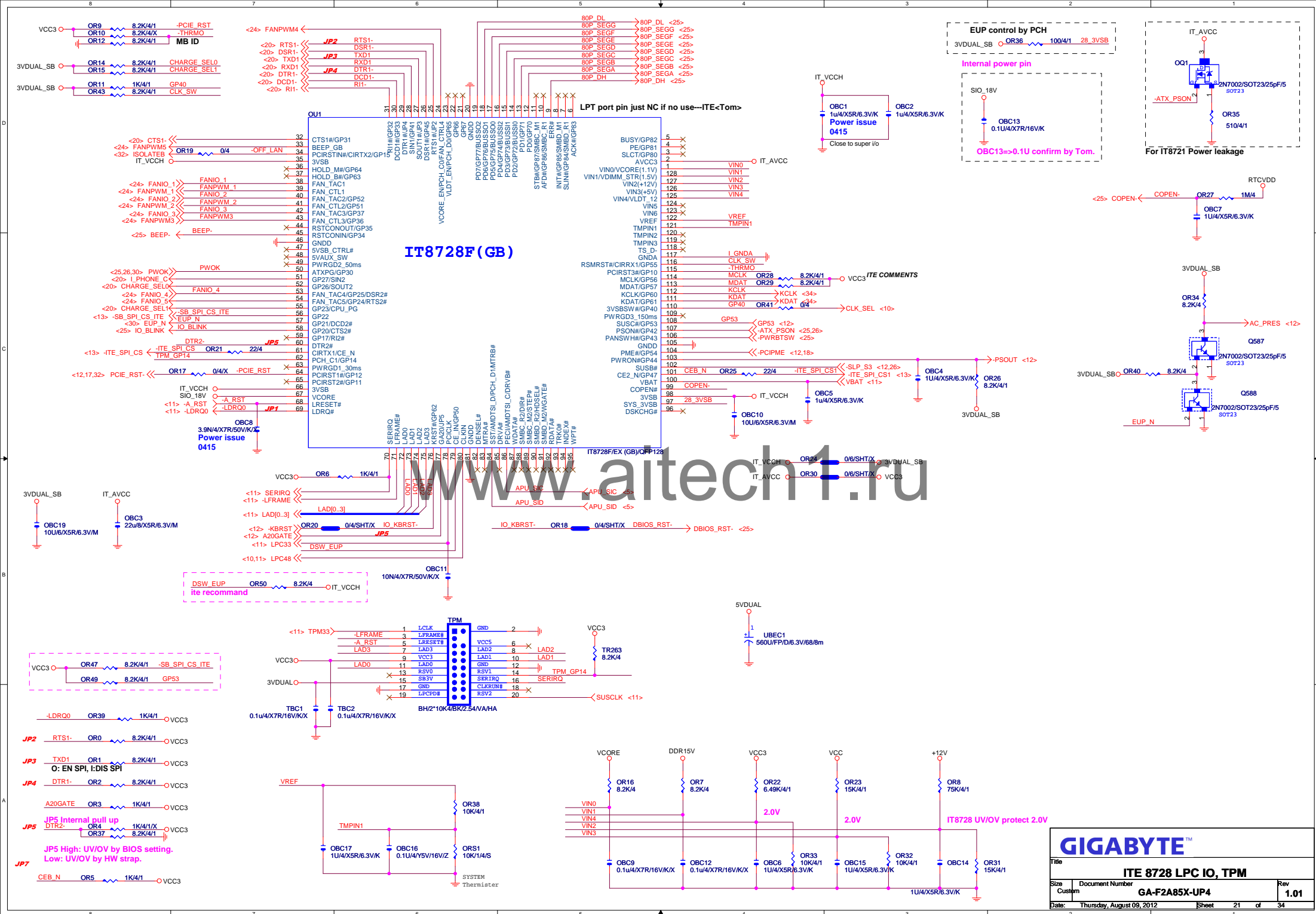
of
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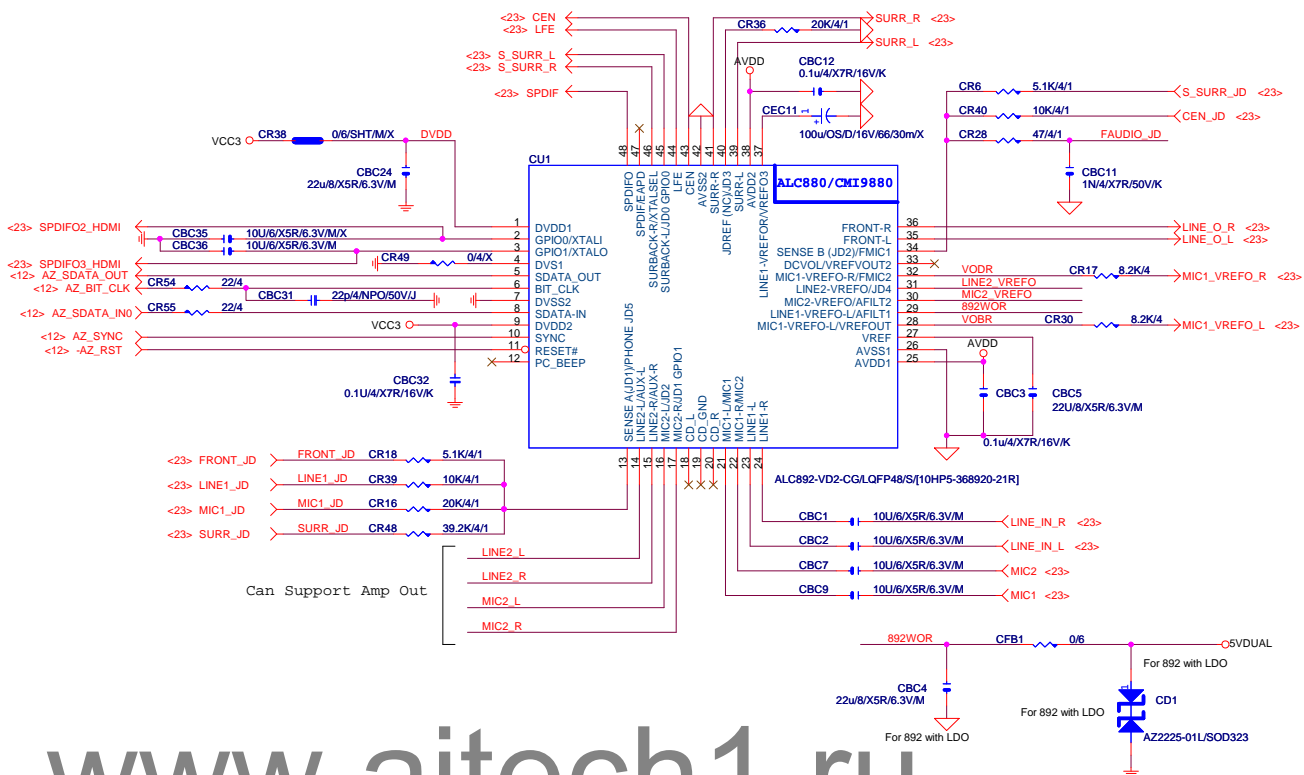




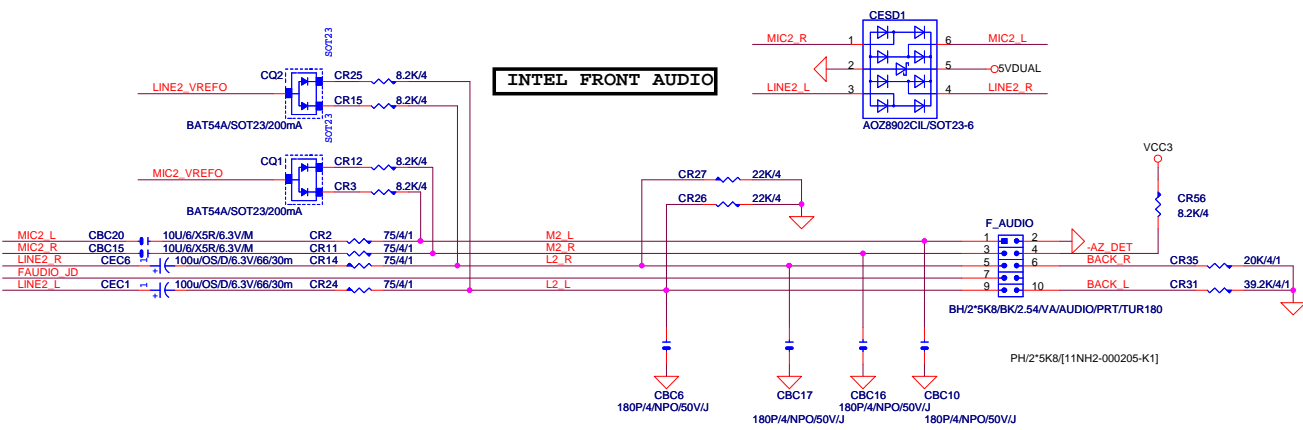




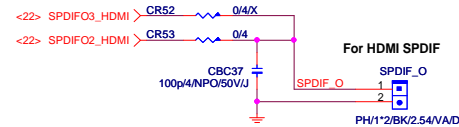
	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



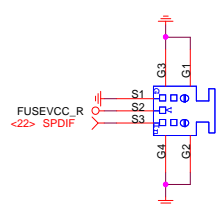
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SPDIF

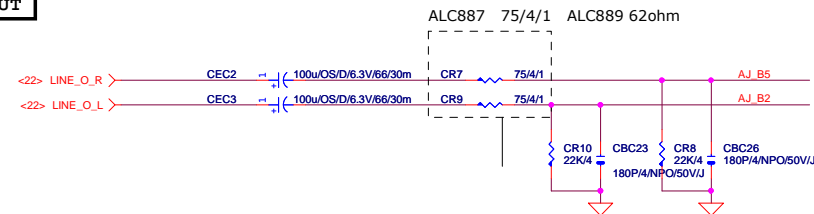


DP_HDMI_SPDIFC

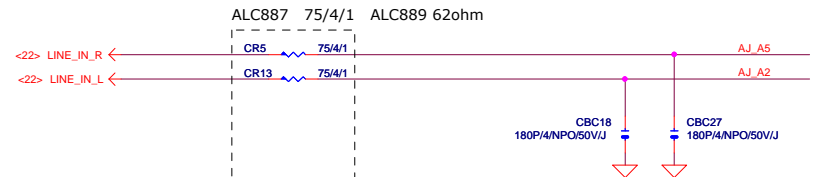


DP+HDMI+SPDIF/20P+19P+3P/BK/RA:DP_HDMI_SPDIF

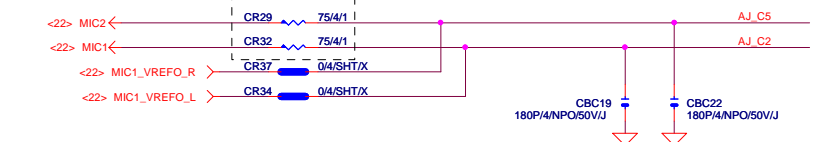
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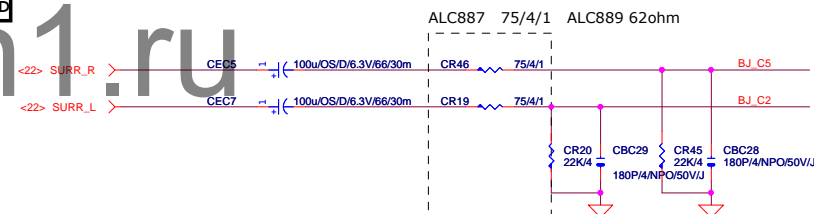
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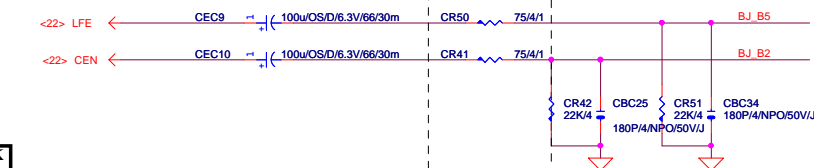
MIC



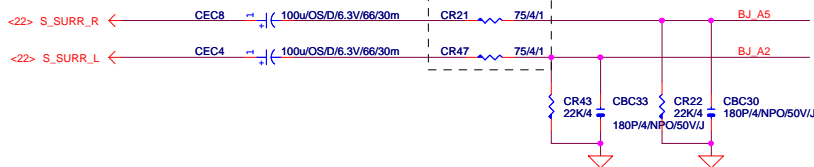
SURROUND



CEN/LFE



SURR BACK

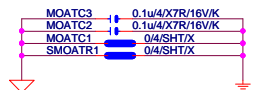
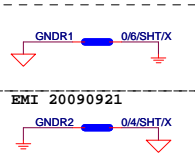
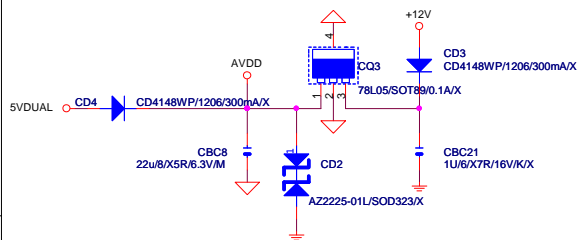


GIGABYTE

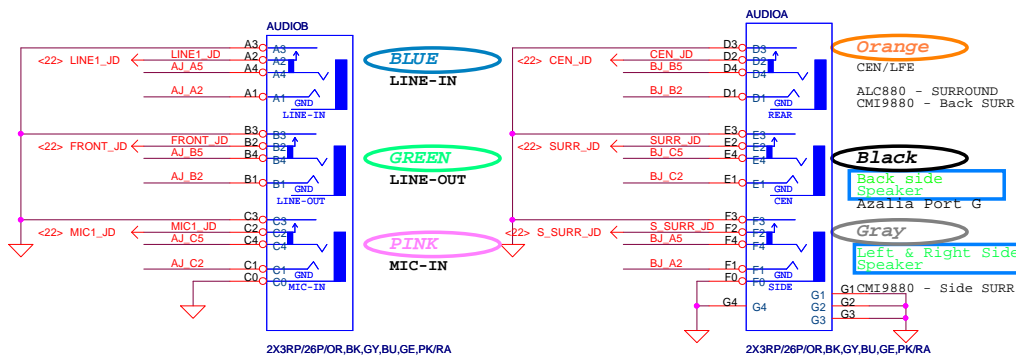
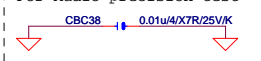
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AUDIO JACK			
Size	Document Number		Rev
Custom	GA-F2A85X-UP4		1.01
Date:	Thursday, August 09, 2012	Sheet	23 of 34

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For ESD PROTECT DIODE



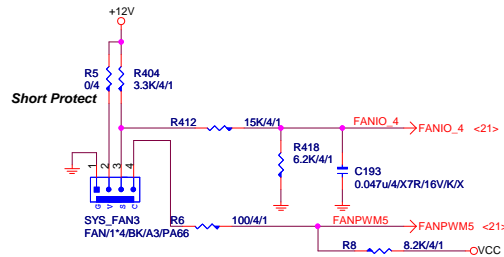
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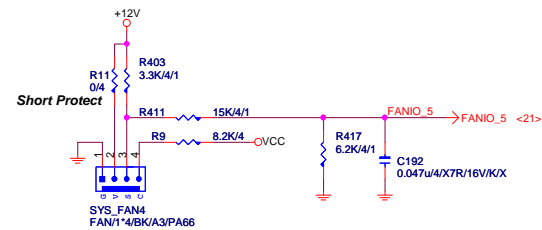
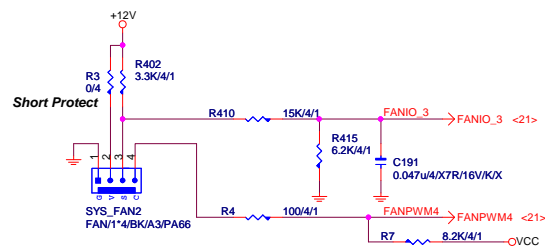
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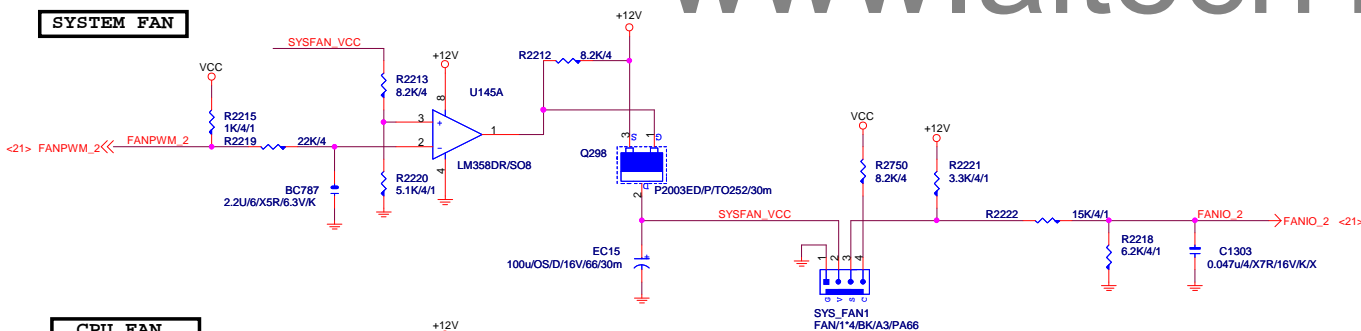
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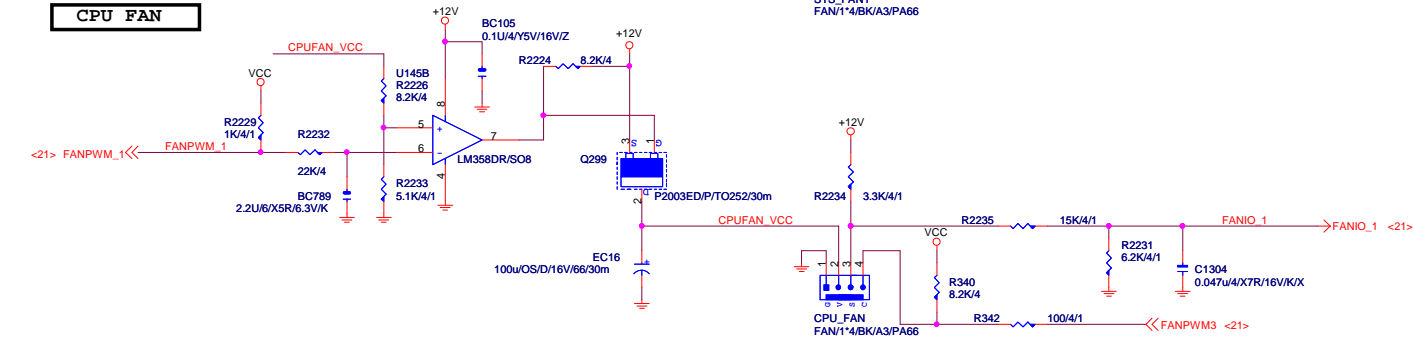
SYSTEM FAN2



SYSTEM FAN

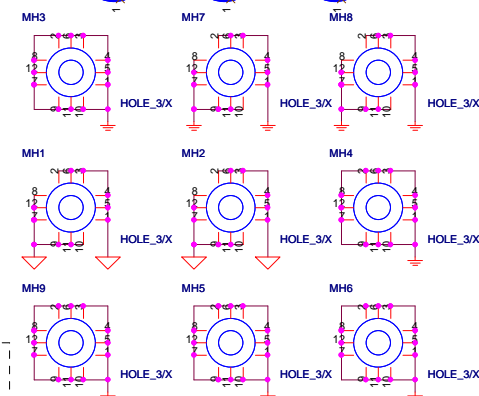
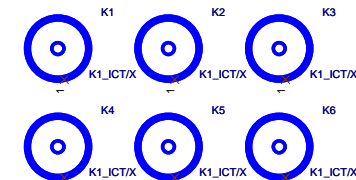
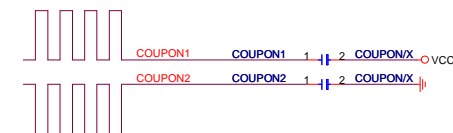
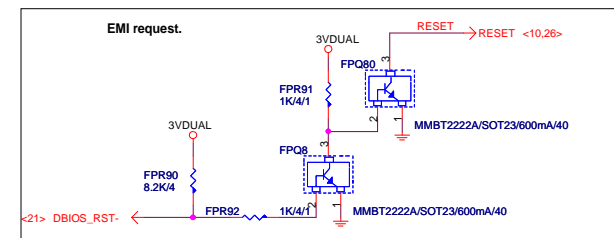
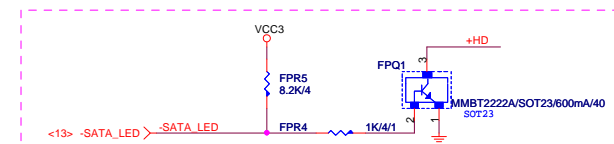
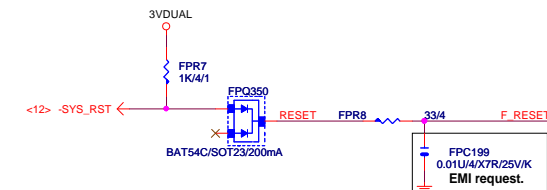
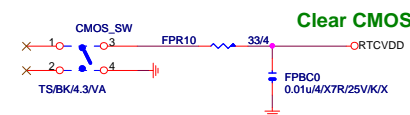
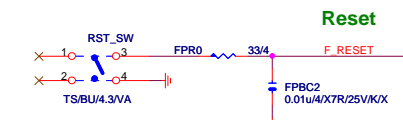
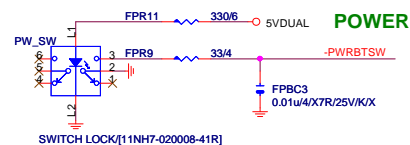
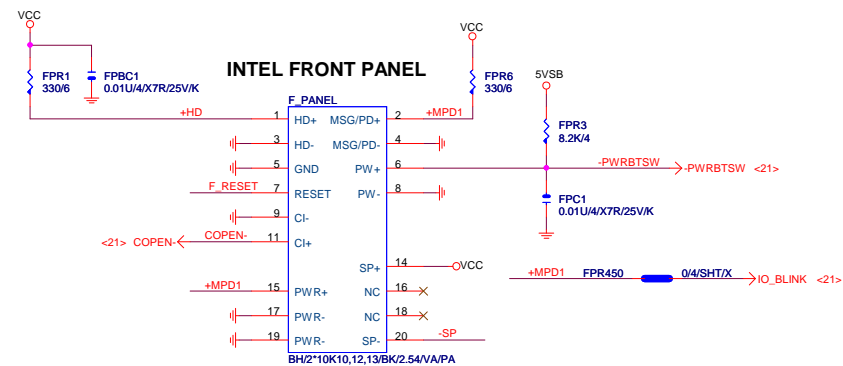


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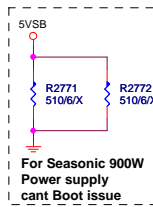
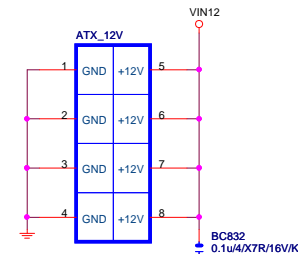
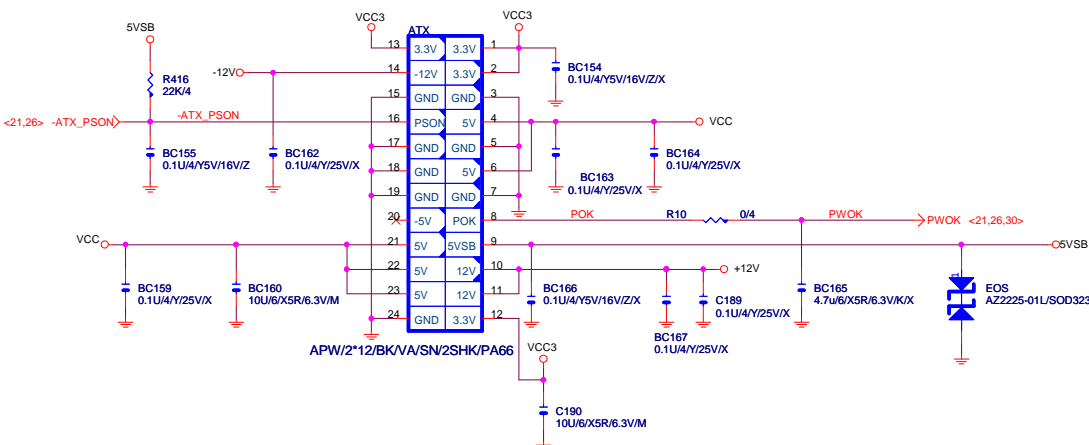


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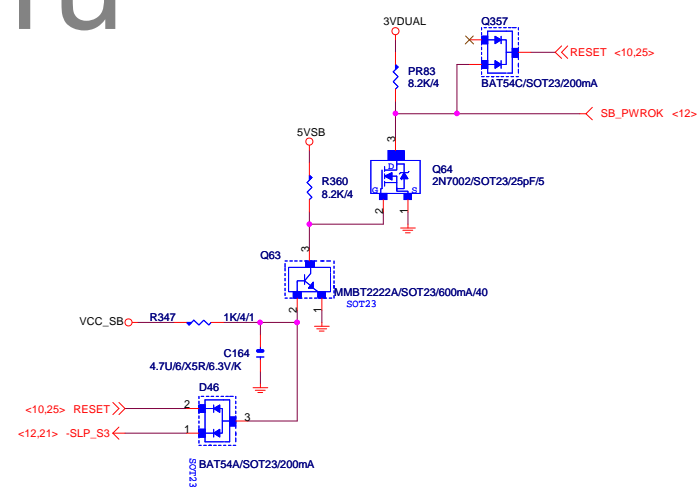
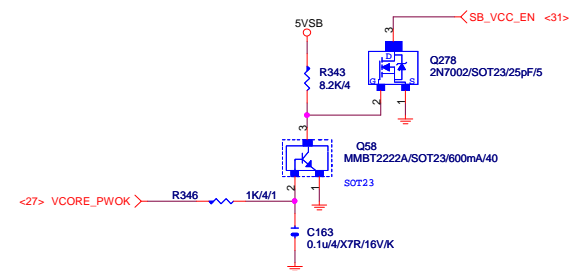
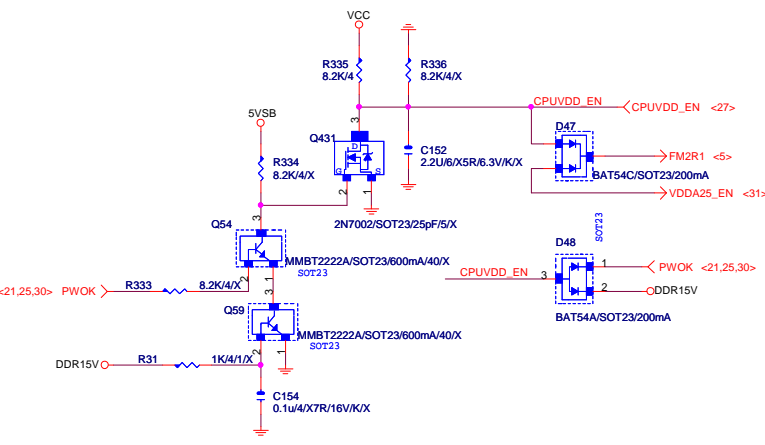
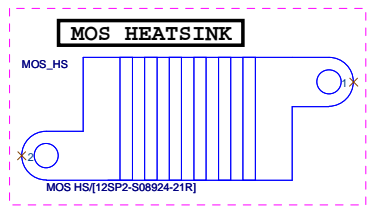
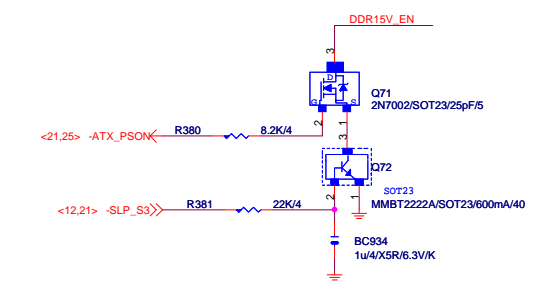
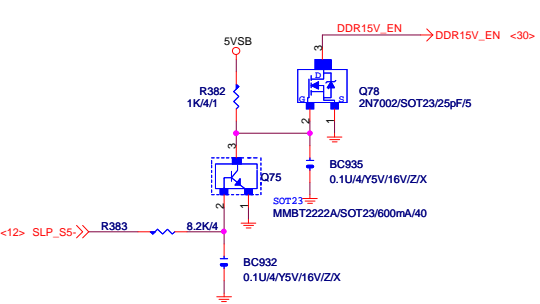
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Size	Document Number	Rev
Custom	GA-F2A85X-UP4	1.01
Date:	Thursday, August 09, 2012	Sheet 24 of 34



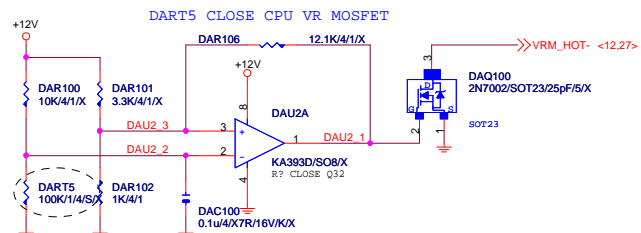
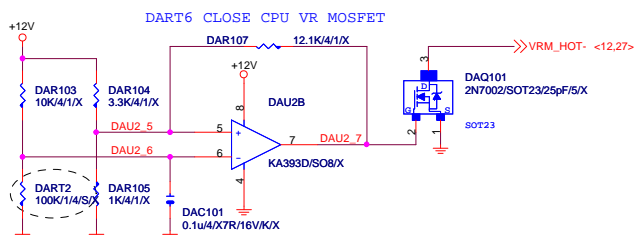
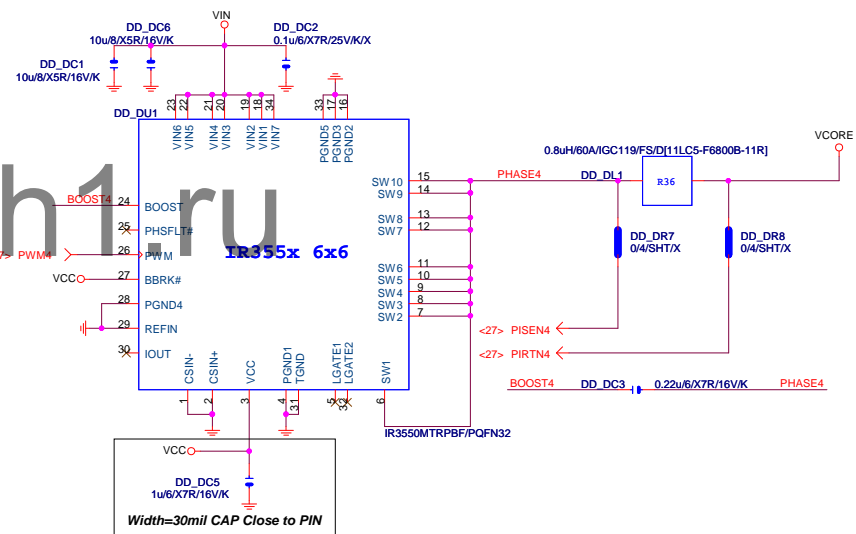
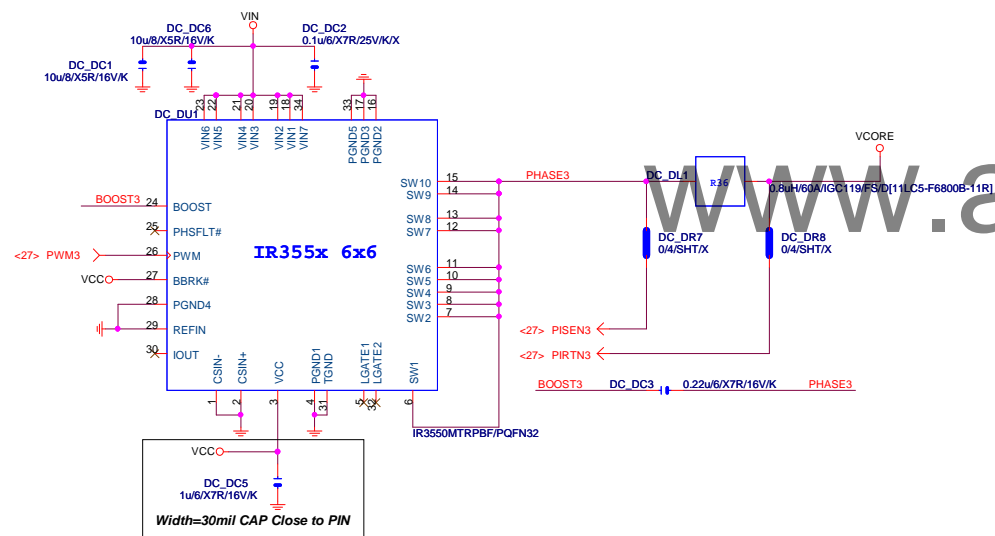
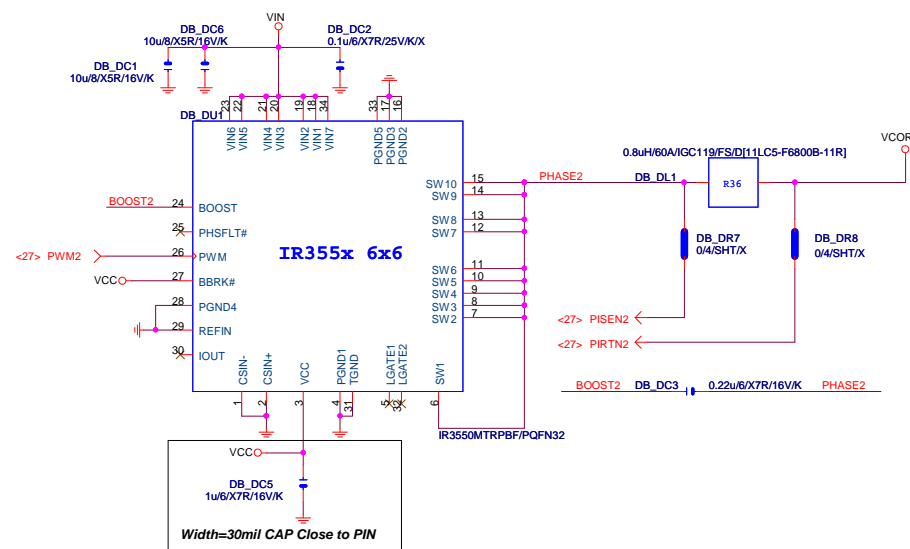
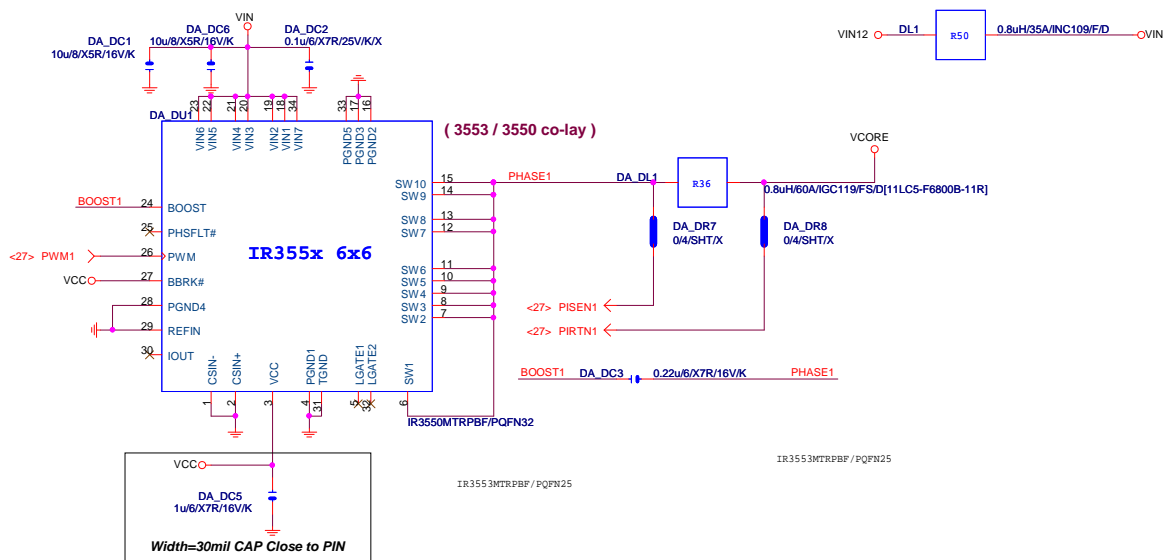
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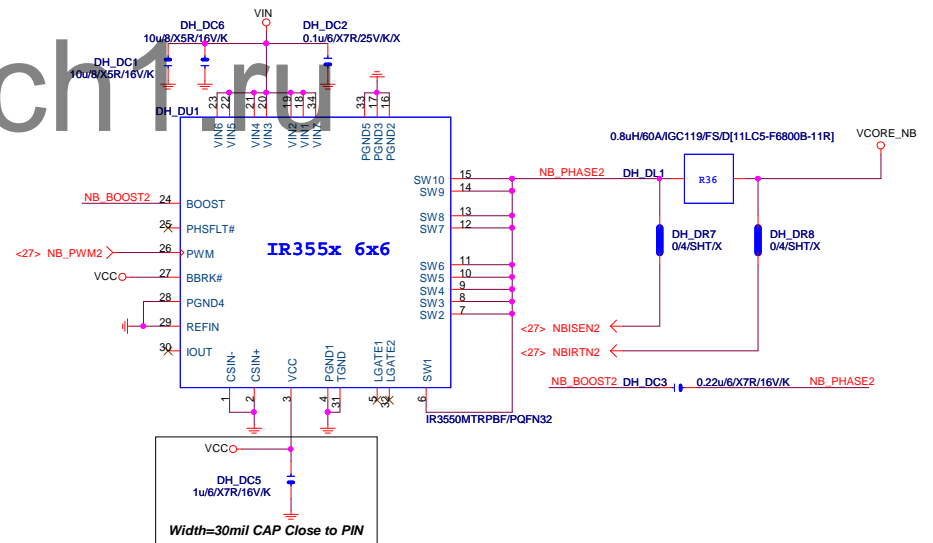
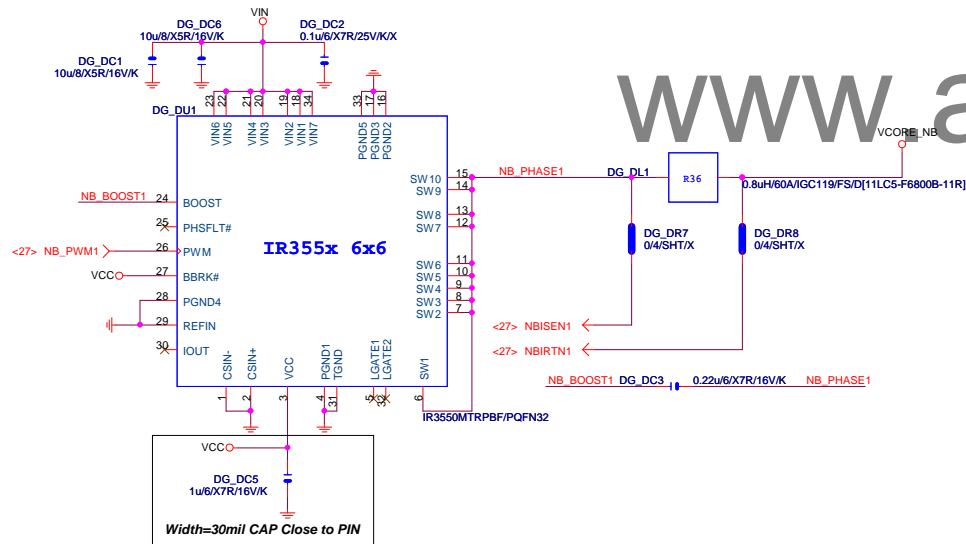
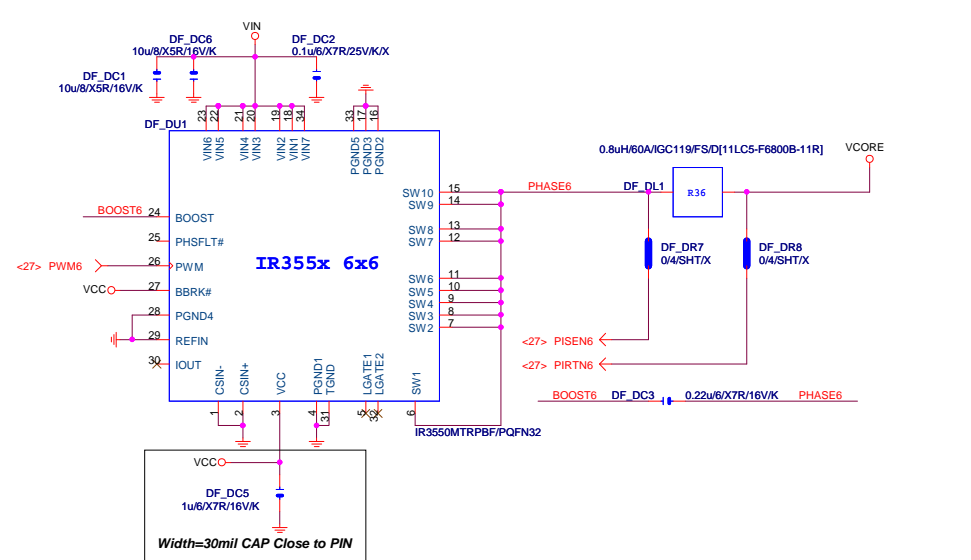
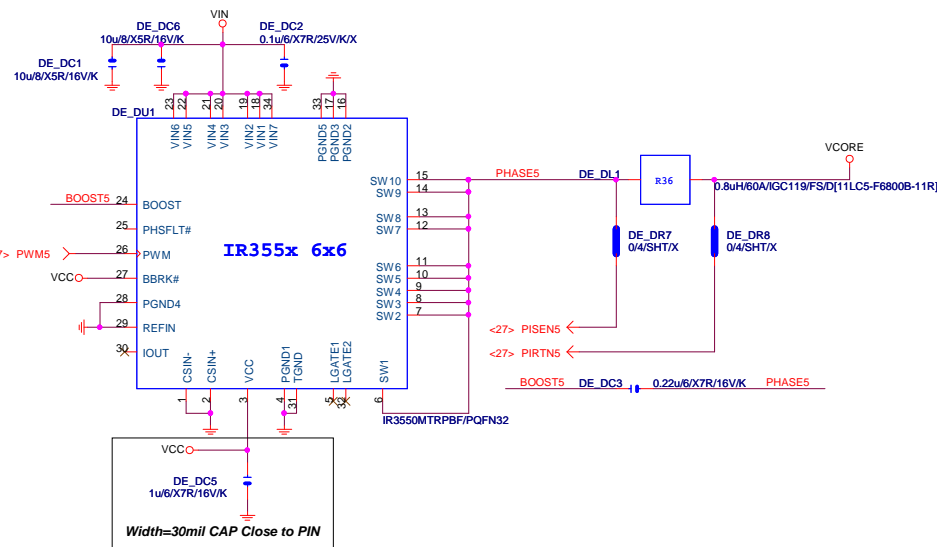
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VCORE MOSFET		
Title	Document Number	Rev
	GA-F2A85X-UP4	1.01
Date	Thursday, August 09, 2012	Sheet 28 of 34

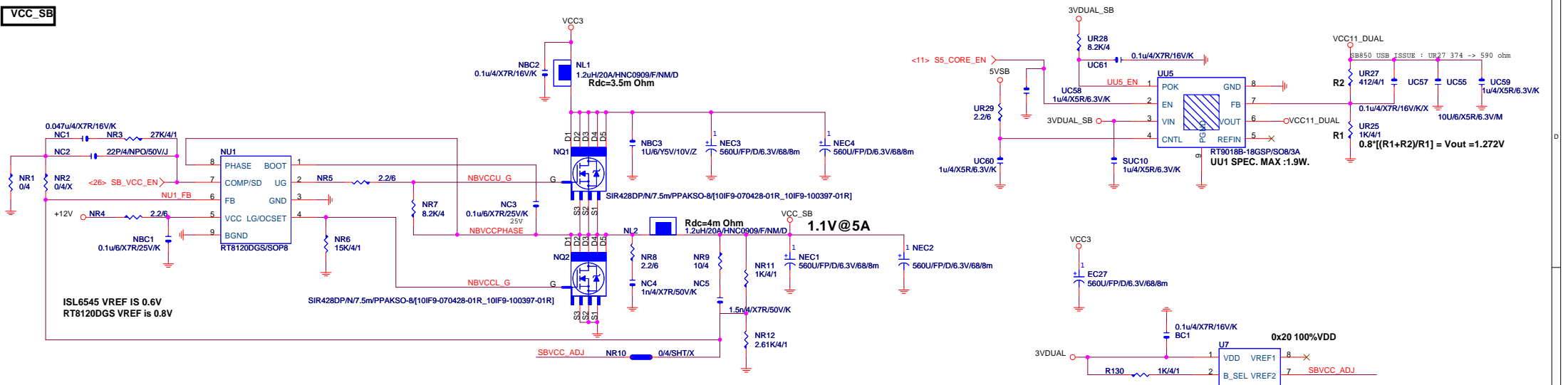
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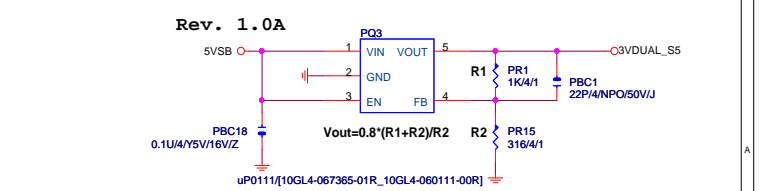
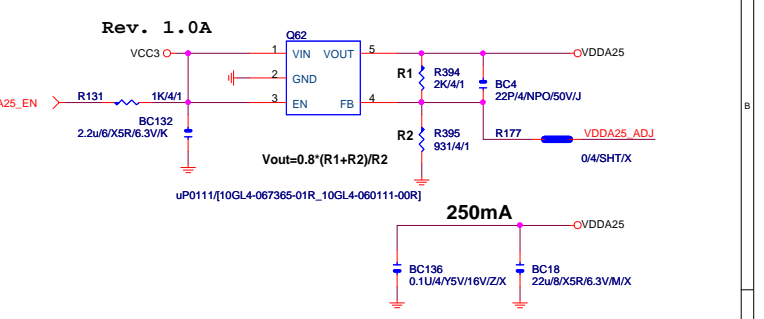
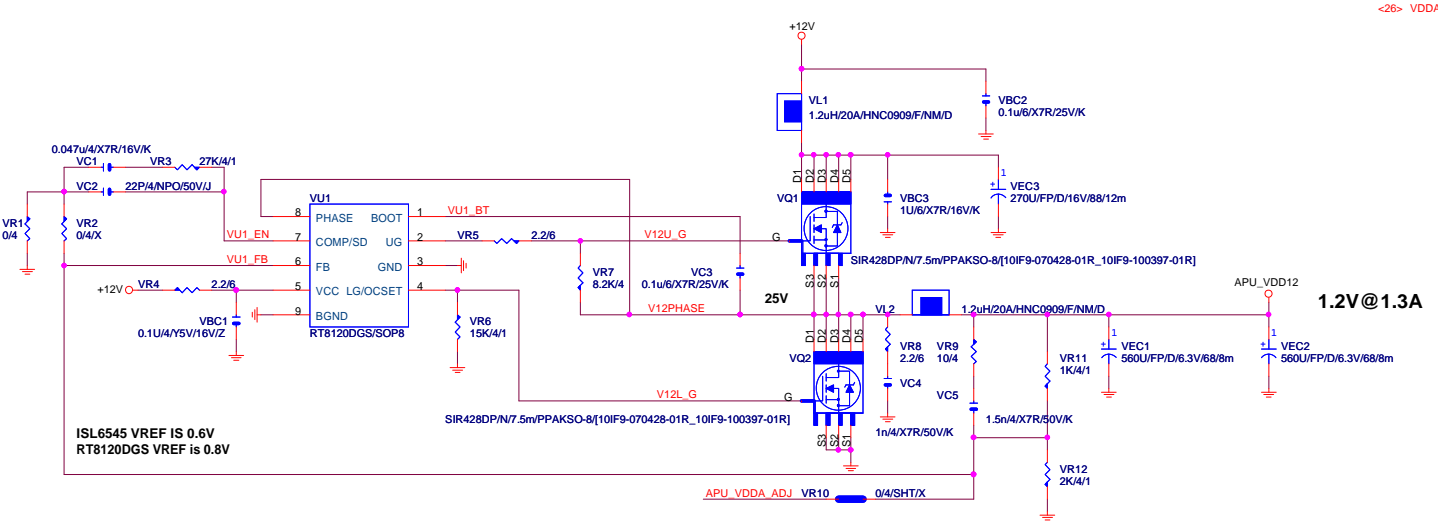
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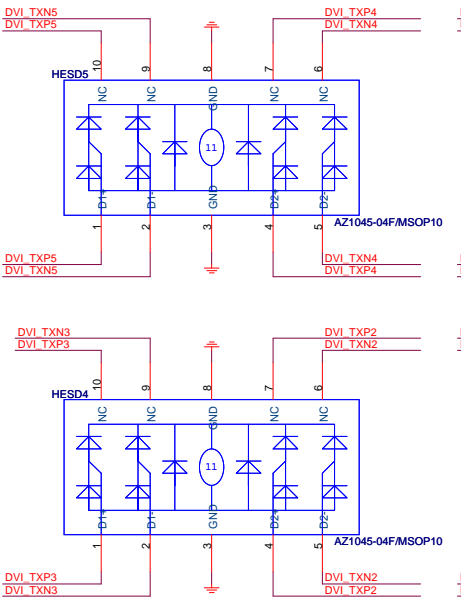
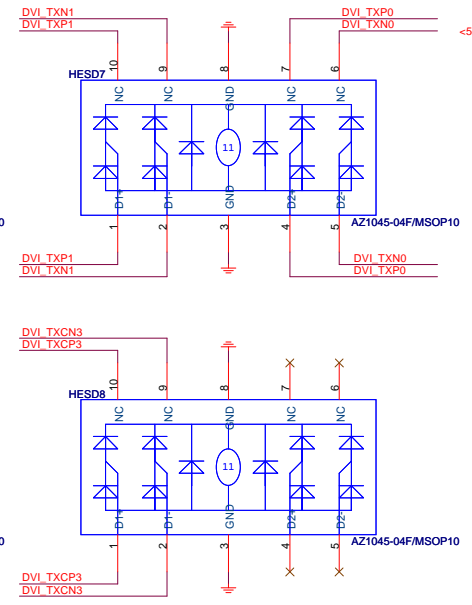
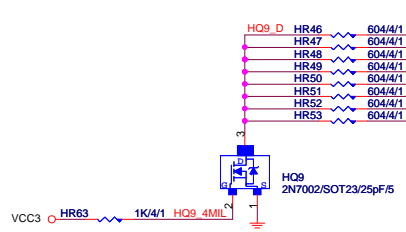
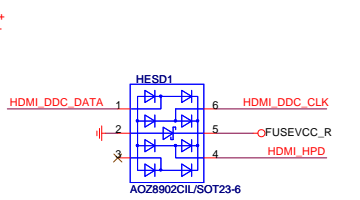
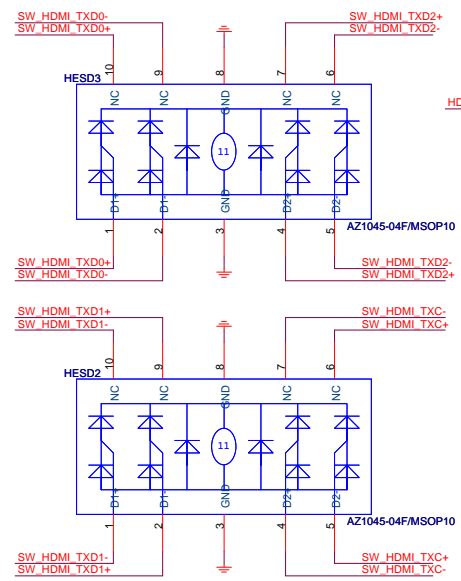
Title			VIA VT6308P
Size	Document Number	Rev	
Custom	GA-F2A85X-UP4	1.01	
Date:	Thursday, August 09, 2012	Sheet	29 of 34

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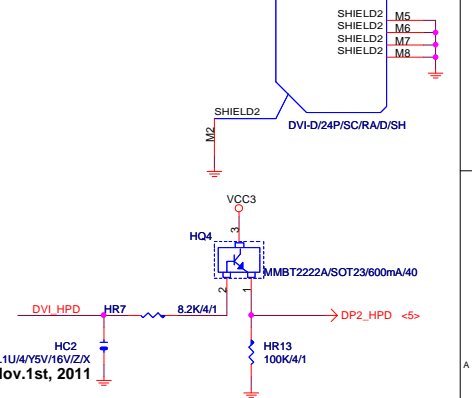
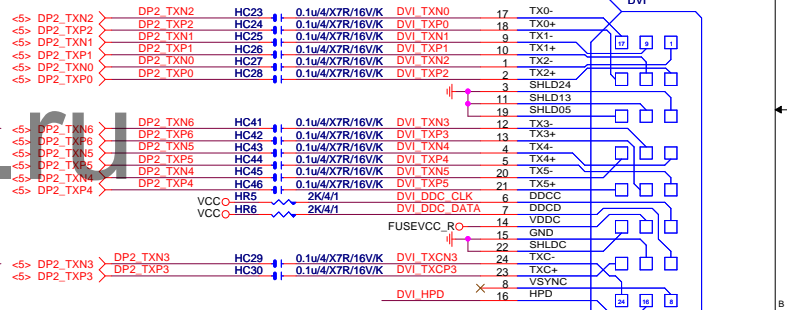
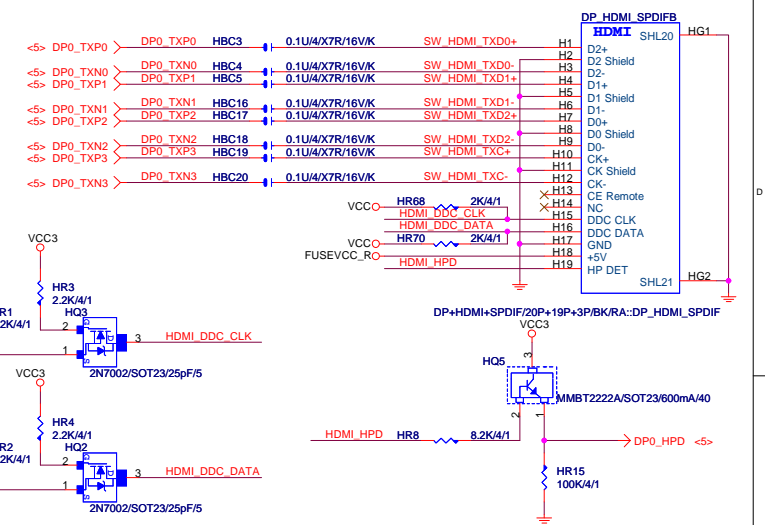
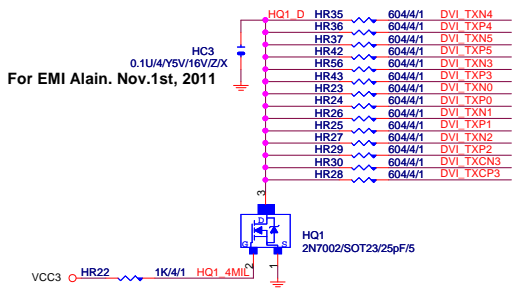
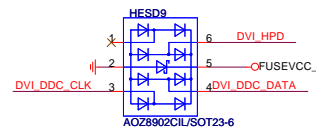
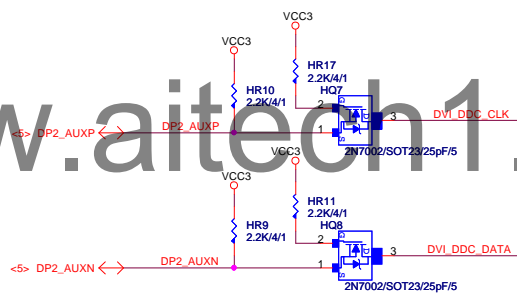


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Title: REALTK RTL8111E-VL		
Size: Custom	Document Number: GA-F2A85X-UP4	Rev: 1.01
Date: Thursday, August 09, 2012	Sheet: 33	of 34

